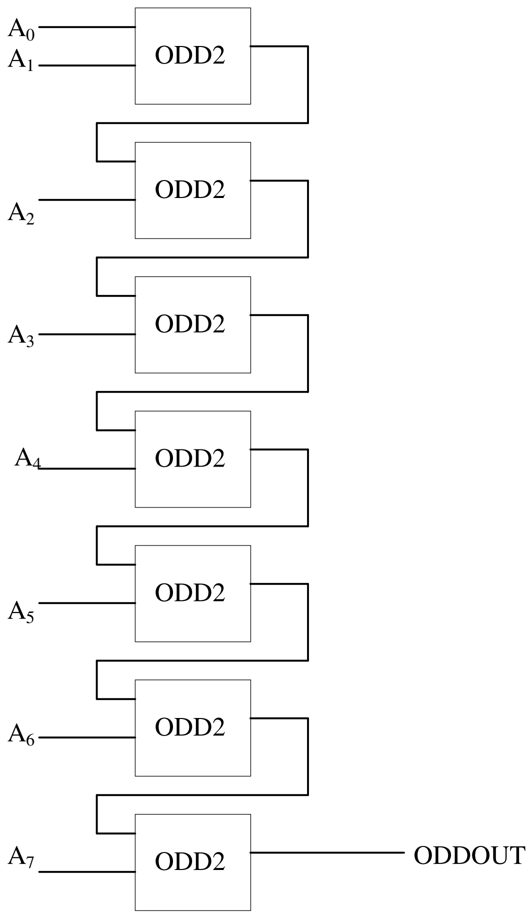
**EECS 150**
**Problem Set 2 Solutions**
**Fall 1999**

**1.**
a) For two single bit inputs X and Y, the odd parity ODD2 is:

| X | Y | ODD2 |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

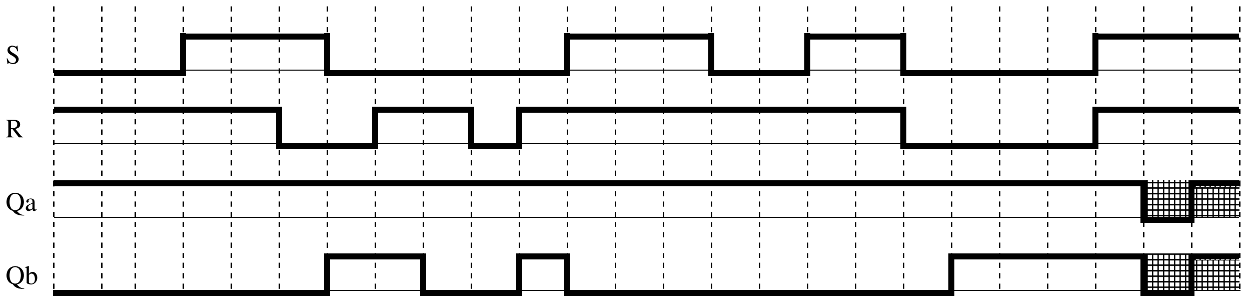
This is just an XOR.

b)




c) Maximum delay comes when input A transitions from $00000000_2$ to $11111110_2$ causing a propagation through all 7 ODD2 modules. ($11111111_2$ will not cause the first ODD2 module to transition since its output would remain 0.) Since each ODD2 module is just an XOR with 3 unit delays, the total is 7*3=21 unit delays.

**2.**

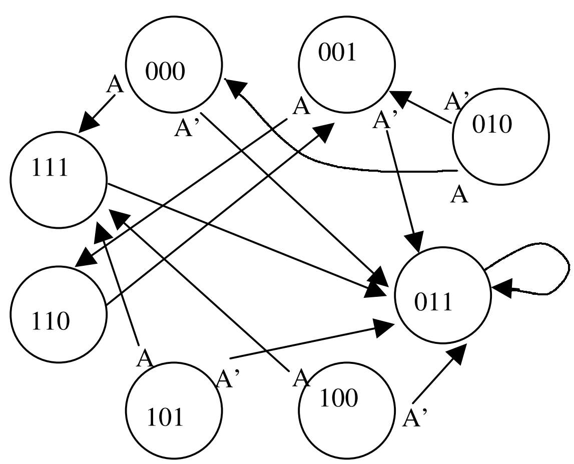



Note that the final transition of S and R high leaves Qa and Qb oscillating.

**3.** State transition table. (Note: A' means "not A")

| $Q_2$ | $Q_1$ | $Q_0$ | A | $D_2 = Q_1$'A | $D_1 = Q_1' + Q_0$ | $D_0 = A' + (Q_1' \text{ xor } Q_0) + Q_2$ |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| 0 | 0 | 1 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 1 | 1 | 1 | 0 |
| 0 | 1 | 0 | 0 | 0 | 0 | 1 |
| 0 | 1 | 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| 0 | 1 | 1 | 1 | 0 | 1 | 1 |
| 1 | 0 | 0 | 0 | 0 | 1 | 1 |
| 1 | 0 | 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 1 | 0 | 0 | 1 | 1 |
| 1 | 0 | 1 | 1 | 1 | 1 | 1 |
| 1 | 1 | 0 | 0 | 0 | 0 | 1 |
| 1 | 1 | 0 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 | 0 | 1 | 1 |
| 1 | 1 | 1 | 1 | 0 | 1 | 1 |

State transition diagram:

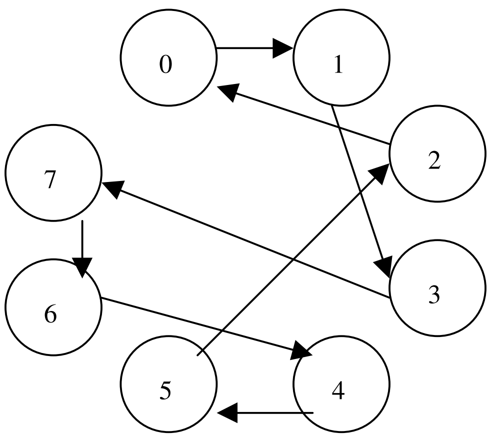


**4.**

State transition table:

| $Q_2$ | $Q_1$ | $Q_0$ | $D_2$ | $D_1$ | $D_0$ |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 | 1 | 1 |
| 0 | 1 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 | 0 | 1 |
| 1 | 0 | 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 | 1 | 0 |

State transition diagram:




To get the needed logic, write the Karnaugh maps for $D_0$, $D_1$ and $D_2$:

$D_0$:

| $Q_2$ \ $Q_1Q_0$ | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 0 | 1 | 1 | 1 | 0 |
| 1 | 1 | 0 | 0 | 0 |

$Q_0$ spans columns 01 and 11; $Q_1$ spans columns 11 and 10.

Therefore, $D_0 = Q_0'Q_1' + Q_0Q_2'$

$D_1$:

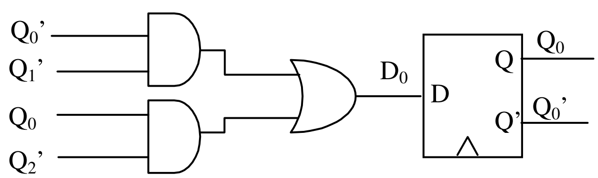
| $Q_2$ \ $Q_1Q_0$ | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 0 | 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 1 | 0 |

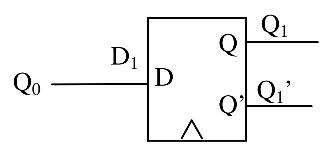
Therefore, $D_1 = Q_0$

$D_2$:

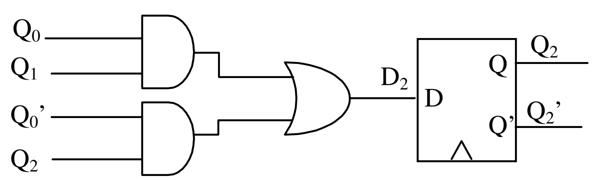
| $Q_2$ \ $Q_1Q_0$ | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 0 | 0 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 | 1 |

Therefore, $D_2 = Q_1Q_0 + Q_0'Q_2$



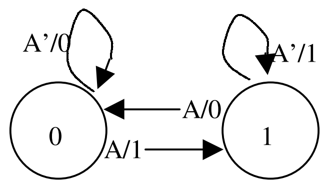




(To keep the schematic neat, just label the wires for $Q_0$ etc., but don't draw them all the way back to the inputs.)



**5.**

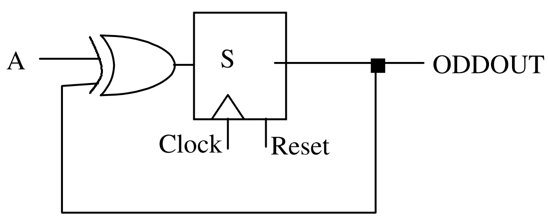
a) Mealy type FSM, following fig. 8.25 in the text.



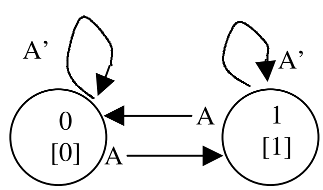

State transition table for the next state $S^+$ based on previous state S and inputs:

| S | A | $S^+$ | ODDOUT |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 0 |

Notice that ODDOUT = $S^+$ and also $S^+$ = S xor A.




b) Moore type FSM, following fig. 8.25 in the text.




Because the output ODDOUT does not depend on the input A in the Mealy type FSM, we end up with the same state diagram for the Moore type FSM. The state transition table and logic diagram are the same.

c) Assume negative clock-edge triggered state register. A is presented most significant bit first.