Professor Fearing EECS150/Problem Set 2 Fall 1999

Due at 10 am, Fri. Sep. 10 in box outside 218 Cory Hall

Reading Katz: 6.1, 8.2, 8.4, 8.5

1. Combinational Logic Design (10 pts)

a. Design a combinational circuit that will take an 8 bit number $A[7:0]$ and determine if A has an odd number of ones. For example if $A = 01110001_2$, then $ODDOUT = 0$. The circuit is built from a 1 bit module which should be cascadable.

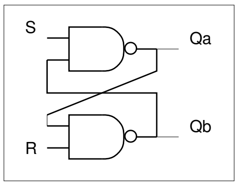
a) Show the truth table for the single bit module.

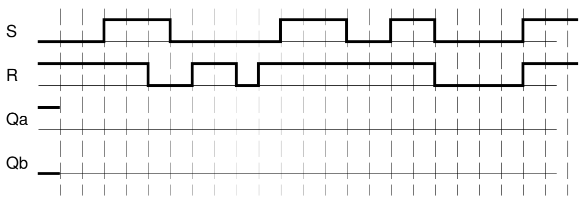
b) Show how the 1 bit modules would be interconnected, using only wires, but no extra gates or inverters to create an 8 bit odd-parity checker.

c) Determine the maximum delay, assuming 1 unit delay for NOT/NAND/NOR, 2 unit delay for AND/OR and 3 unit delay for XOR/XNOR.

2.Set-Reset Latch Timing (20 pts)

Complete the timing diagram for the latch below, assuming unit delay through the gates. The grid spacing is one unit delay.





3. Finite State Machine Analysis (25 pts)

Make a state transition table and state diagram for an FSM with a state register consisting of three D type FF, and input signal A. The next state equations (equivalently, inputs to the FF) are:
$D_0 = \bar{A} + \bar{Q}_1 \oplus Q_0 + Q_2, \quad D_1 = \bar{Q}_1 + Q_0$, and $D_2 = \bar{Q}_1 \cdot A$.

4. Counter Design (20 pts)

Using 3 type D flip-flops and extra logic, design a 3 bit counter which counts in the sequence $Q_2Q_1Q_0 = 0, 1, 3, 7, 6, 4, 5, 2, 0, \ldots$. Show state diagram, state transition table and schematic diagram.

5. FSM Design (25 pts)

This problem examines a sequential logic approach to the parity function described in problem 1. The finite state machine has as inputs a synchronized serial bit stream A, presented with most significant bit first. At each clock, the output of the FSM should be 1 if an odd number of ones have been read, and 0 if an even number of ones have been read.

a) Draw a state diagram, state table, and logic diagram for a Mealey type FSM which implements this function. You will probably need a global reset signal to initialize the FSM.

b) Draw a state diagram, state table, and logic diagram for a Moore type FSM which implements this function. You will probably need a global reset signal to initialize the FSM.

c) Draw a functional timing diagram showing A, clock, $ODDOUT$ for the input $A = 11010001$ for the Moore and Mealey FSMs.