Professor Fearing EECS150/Problem Set 10 Fall 1999

Due at 10 am, Fri. Nov. 19 in box outside 218 Cory Hall

(This problem set may be done individually or by a group of two people maximum.)

1. K-maps (40 pts)

With a four digit binary input number $A_3A_2A_1.A_0$, design a circuit that generates a 4 bit output code $BC.DE_2$ which is the square root of the input. For example if the input is 4 (100.0_2), $\sqrt{4} = 10.00_2$ thus the four output functions should be $B = 1$, $C = 0$, $D = 0$, and $E = 0$. The inputs and outputs are Asserted High.

- Define the truth table for the four functions.
- Show all Karnaugh maps for S.O.P. and P.O.S.
- Draw the logic diagram using NAND gates only for minimized S.O.P. (Follow the bubble matching conventions).
- Draw the logic diagram using NOR gates only for minimized P.O.S. (Follow the bubble matching conventions).

2. State Minimization (30 pts)

Given the state diagram of Figure Ex9.2 (Katz pg. 488), use the state implication method to find and draw the fully reduced state diagram.

3. Coupled Mealey Machines (30 pts)

You are given a schematic for a counter using an X74163. The ENP and ENT inputs are tied together, the data inputs are tied to $DCBA = 1000$. A Mealy machine with two states is used to control the counter. In the WAIT state, the Mealy FSM continuously loads the counter, and waits for a signal START, then goes to the COUNT state and asserts ENP/ENT until RCO is asserted then returns to the WAIT state.

a. Use a timing diagram to show how these coupled Mealy machines could get confused. (Hint: RCO is a Mealy output).

b. Fix the circuit so it functions as intended.