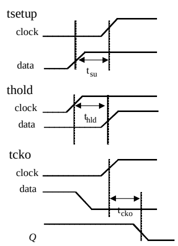
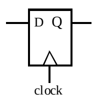
0 Admin
1 What to do about wires?
2 Tri-state gates
3 Bus example with timing

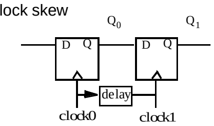
1 RECAP

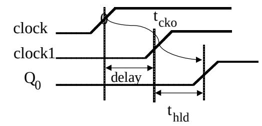




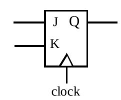
1 RECAP (cont.)

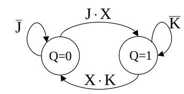
Clock skew





Okay if t_{cko} > delay + t_{hold}

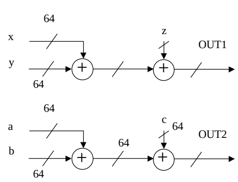




2 WHAT TO DO ABOUT WIRES?

Example: out1 = x + y + z; long 64 bits x,y,z
out2 = a + b + c; a,b,c

2a. Full-parallel implementation



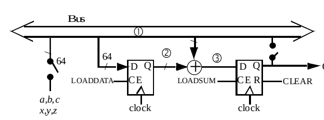
2 WHAT TO DO ABOUT WIRES (cont.)

2a.1 Cost of implementation

6 input busses, 2 internal busses, 2 output busses, 640 wires

delay: 2 adder delays "$2 \cdot T_{add}$"

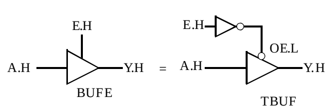
2b. Sequential approach



(Time Division MUX)
1 input bus, 3 internal busses, 1 output bus (256 wires)
2 switches, 2 regs, 1 adder

How to implement switch?

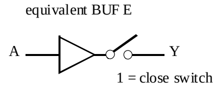
3 TRI-STATE GATES



Truth table

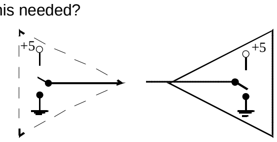
E.H	A	Y	
0	0	Hi-z	"tri-state"
0	1	Hi-z	
1	0	0	enabled
1	1	1	

equivalent BUF E



3 TRI-STATE GATES (cont.)

Why is this needed?

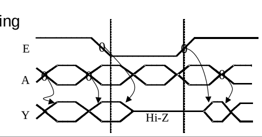


gates would fight inside chip

bad because: (1) indeterminate level

(2) over-heating

3.1 Timing

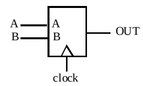


4 BUS EXAMPLE WITH TIMING

Algorithm given: while (1)
{out = A; wait(); out = B; wait();}

input A,B, output OUT

single bit, output latched



Method
1 block diagram (detail)
2 timing
3 state diagram, etc.

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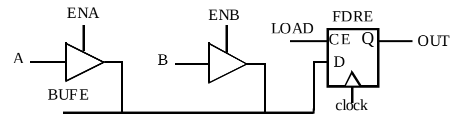
4 BUS EXAMPLE WITH TIMING (cont.)

4.1 Block Diagram



Register transfer language/notation

Now design timing to avoid bus conflicts

$A \rightarrow OUT:\ ENA, LOAD, \overline{ENB}$

$B \rightarrow OUT:\ ENB, LOAD, \overline{ENA}$

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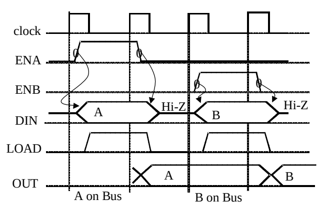
4 BUS EXAMPLE WITH TIMING (cont.)

4.2 Timing



Note: Delays included

Wait prevents bus contention due to skew

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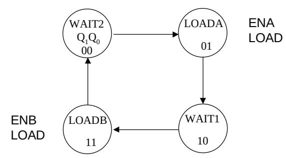
4 BUS EXAMPLE WITH TIMING (cont.)

4.3 State Diagram – How many states? 4



Use 2-bit CTR

$LOAD = Q_0$

$ENB = Q_0 \cdot Q_1 \qquad ENA = \overline{Q}_1 \cdot Q_0$