

0 Admin
1 Recap
2 D FF timing
3 Toggle and JK FF

1 RECAP

- X74_163 synchronous counter
- FSM using counters

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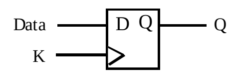
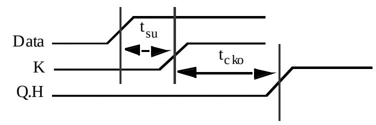
2 D FF Timing



Setup time: min time before K for data to be valid



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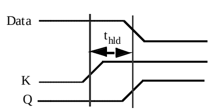
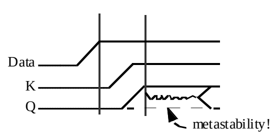
2 D FF Timing (cont.)

Hold Time

T_{hld} = min time after K for which data must remain valid



What happens if setup and/or hold is violated? Indeterminate



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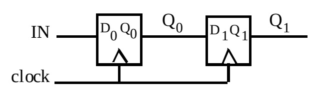
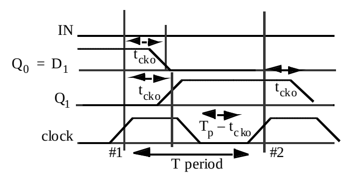
2 D FF TIMING (cont.)

2.1 Shift Register Revisited





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2 D FF TIMING (cont.)

2.1.1 Timing Constants for Shift Register

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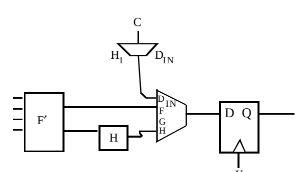
2 D FF TIMING (cont.)

2.2 Xilinx Timing (4005_4)

Shift register holdtime 0 min
t_{cko} 3.7 ns
setup time D_{in}
t_{Dick} 3.0 ns
F′/G′ and H′
t_{1Hck} 6.1 ns



2 D FF TIMING (cont.)

2.2 Xilinx Timing (cont.)

How fast can it run?

$$\frac{1}{\text{min clock period}} = \frac{1}{t_{cko} + t_{setup}}$$

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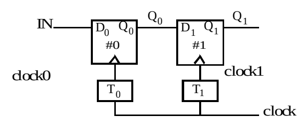
2 D FF TIMING (cont.)

2.3 Clock Skew



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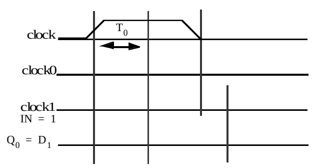
2 D FF TIMING (cont.)

2.3 Clock Skew (cont.)



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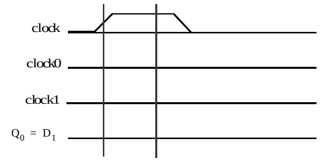
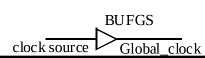
2 D FF TIMING (cont.)

2.3 Clock Skew (cont.)





limit 4

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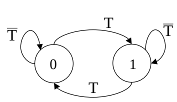
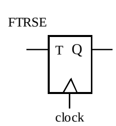
3 OTHER FF TYPES

Toggle Flip Flop





Convert D to T

T	PS	NS
0	0	0
0	1	1
1	0	1
1	1	0

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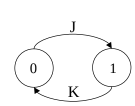
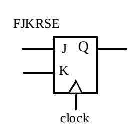
3 OTHER FF TYPES (cont.)

JK FF

J	K	Q_{n+1}	Comment
0	0		
0	1		
1	0		
1	1		





Convert D to JK

J	K	Q_n	Q_{n+1}
0	0		
0	0		
0	1		
1	0		
1	1		
1	1		