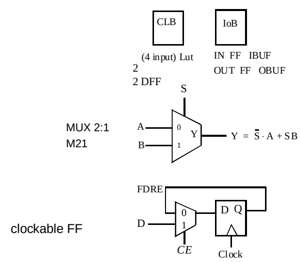
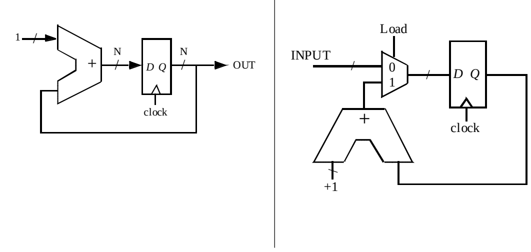
0 Admin
1 Recap
2 Loadable counter
3 Design example: Walk light

1 RECAP – Xilinx FPGA



2 LOADABLE COUNTER

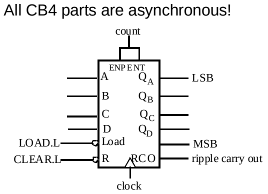
For (i = 0, i < N; i++)



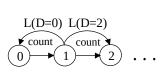
2 Loadable Counter (cont.)

2.1 Xilinx library part ×74_163 (note: synchronous clear)

Note: All CB4 parts are asynchronous!

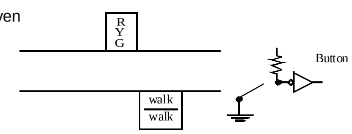


2.1.1 State diagram – very flexible – “branch counter”



3 DESIGN EXAMPLE: Crosswalk Control

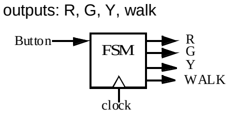
Given



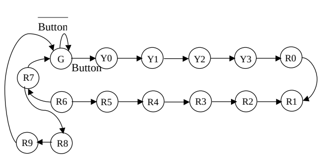
Problem:
Design FSM controller so that traffic light turns yellow when Button asserted. Yellow for 4 sec., Red for 2 sec., then RED and walk for 8 seconds. Given 1 Hz clock. Assume Button synchronized. Use Moore machine.

3 Design Example (cont.)

Step 1. Block Diagram. Inputs?
Button outputs: R, G, Y, walk

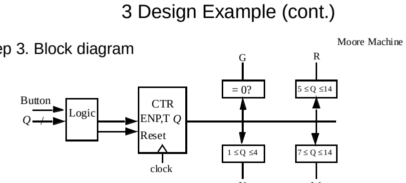


Step 2. State diagram/Moore machine



3 Design Example (cont.)

Step 3. Block diagram



Step 4. State transition table

Button	$Q_3Q_2Q_1Q_0$	ENP,T	Reset.L	Comment
0	0	0	0	hold
1	X	1	0	
0	0001…1101	1	0	
X	111X	1	1	reset

$ENP = Button + Q_3 + Q_2 + Q_1 + Q_0$, $RESET.L = Q_3 \cdot Q_2 \cdot Q_1$

CLB estimate - output decoders 2 CLB/input logic probably merged into CLB

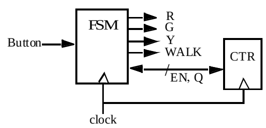
CTR ~ 4 CLB

3 Design Example (cont.)

3.2 Alternate Design

Illustrates: Almost one hot encoding ⇒ glitch-free outputs
Eliminate output decoders – fewer CLBs for logic
combining FSMs ⇒ more CLBs for FF

Step 1. Block diagram



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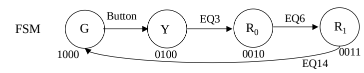
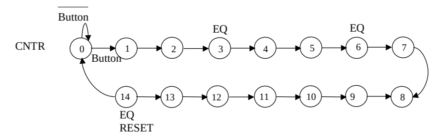
3 Design Example (cont.)

No unique solution – always different tradeoffs, time, space, ...

Step 2. State diagram



State assignment G Y R W



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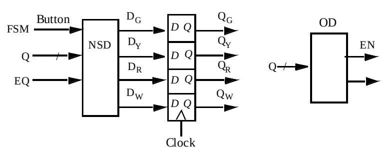
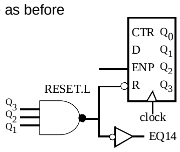
3 Design Example (cont.)

Step 3. Block diagram



same as before



$ENP = \overline{Button} + Q_3 + Q_2 + Q_1 + Q_0$

$RESET.L = Q_3 Q_2 Q_1$

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3 Design Example (cont.)

Step 4. State transition table

IN			PS			NS				Comment
Button	EQ	Q_G	Q_Y	Q_R	Q_W	Q_G	O_Y	Q_R	Q_W	
0	X	1	0	0	0	1	0	0	0	hold
1	X	1	0	0	0	0	1	0	0	g → y
X	0	0	1	0	0	0	1	0	0	hold
X	1	0	1	0	0	0	0	1✓	0	y → r
X	0	0	0	1	0	0	0	1✓	0	hold
X	1	0	0	1	0	0	0	1✓	1	r → w
X	0	0	0	1	1	0	0	1✓	1	hold
X	1	0	0	1	1	1	0	0	0	w → g

Watch out! 12 bogus states:

$$\text{fatal} \begin{cases} 1001 \\ \cdots \\ 1111 \end{cases}$$

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3 Design Example (cont.)

$$D_G = Q_G \cdot \overline{Q}_Y \cdot \overline{Q}_R \cdot \overline{Q}_W \cdot \overline{Button}$$
$$+ EQ \cdot \overline{Q}_G \cdot \overline{Q}_Y \cdot Q_R \cdot Q_W$$

$$D_Y = Button \cdot Q_G \cdot \overline{Q}_Y \cdot \overline{Q}_R \cdot \overline{Q}_W$$
$$+ \overline{EQ} \cdot \overline{Q}_G \cdot Q_Y \cdot \overline{Q}_R \cdot \overline{Q}_W$$

$$D_R = \overline{Q}_G \cdot [\overline{Q}_Y \cdot Q_R \cdot \overline{Q}_W + EQ \cdot \overline{Q}_R \cdot \overline{Q}_W \cdot Q_Y + \overline{EQ} \cdot \overline{Q}_Y \cdot Q_R \cdot Q_W]$$

$$D_W = \overline{Q}_G \cdot \overline{Q}_Y \cdot Q_R(EQ \oplus \overline{Q}_W)$$

Consider alternative state diagrams and block diagrams – final simplest choice: number of FSMs, building blocks, Mealey/Moore that meets specifications