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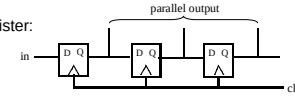
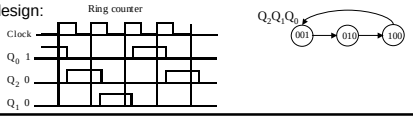
0 Admin
1 Recap
2 Programmable Gate Array
3 CLB
4 IoB
5 Routing Interconnect
6 Design Flow
7 MUX, enable FF

1 RECAP

• Shift register:



•Counter design:



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2 PROGRAMMABLE GATE ARRAY

Motivation: Memory-based logic
- change HW as easily as SW
- density and cost ~ memory cost
- algorithms compiled to HW

HP teramac — 300 megabit "instruction" completely redefines computer on reload

ILIW – "insanely long instruction word" … ~1 msec.

"swap jobs" ⇒ change HW (virtual machines)

10× or 100 × speedup

compile to HW

timesharing

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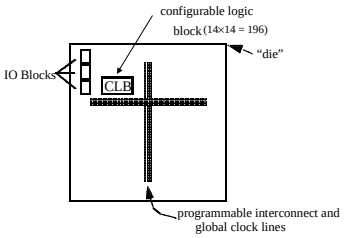
2 Programmable Gate Array (cont.)

2.1 Xilinx 4005 Architecture



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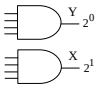
3 CONFIGURABLE LOGIC BLOCK

Look up table (LUT) – 4 inputs, 2 outputs

char lookup [16]={…};

Address	Data 2^1 2^0
0 0 0 0	
.	
.	
.	
1 1 1 1	

Example:



any 2 combined functions of 4 inputs:

0,0,0,0
0,0,0,0
0,0,0,0
0,0,0,3

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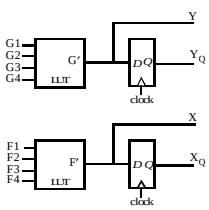
3 Configurable Logic Block (cont.)

Simplified form: One CLB



Either:

2 fcns of 4 vars

or

1 fcn. of 5 vars

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3 Configurable Logic Block (cont.)

LUT can also be used as internal read/write memory

16 × 2 random access memory

Example: Counts

4 bit loadable synchronous counter – 4 CLB

16 bit full adder ~16 CLB, ~50 MHz

Usual limit is routing, not # CLB

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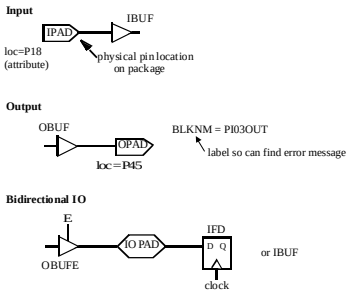
4 INPUT/OUTPUT BLOCK

(Note: only 58 connected)



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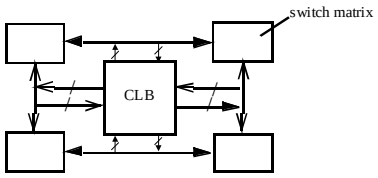
5 ROUTING/INTERCONNECT



For most designs, limitation is interconnect, not number of CLBs.

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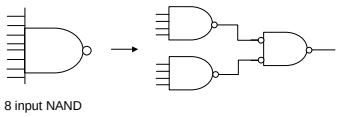
6 DESIGN FLOW

Viewlogic netlist (EDIF)

↓

MAP functions into CLB

For example:



8 input NAND

- Simplifies logic (espresso), removes unused gates, unused inputs, minimizes
- place & route: non-deterministic optimization, simulated annealing

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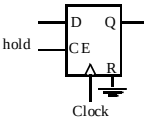
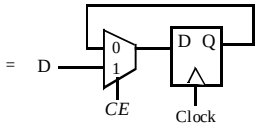
7 CLOCK ENABLE – FF: FDRE

D	CE	Q^+
X	0	Q_n
0	1	0
1	1	1





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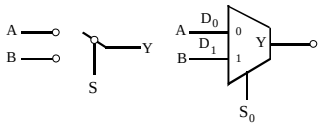
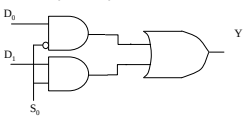
7 Clock Enable (cont.)

Multiplexer: M2_1



If $S_0 = 0$, Y = A

$S_0 = 1$, Y = B

$$Y = \overline{S}_0 \cdot A + S_0 \cdot B$$

D_0	D_1	S_0	Y
D_0	X	0	D_0
X	D_0	1	D_1