0 Admin
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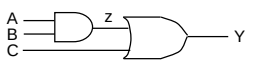
3 IDCT in hardware

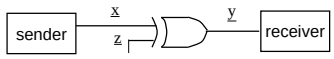
1 RECAP

- Static Fault Testing: test vectors



Node	Test vector A B C
A SA0	1 1 0
A SA1	0 1 0
B SA0	
B SA1	
C SA0	0 0 1
C SA1	0 0 0
Z SA0	1 1 0
Z SA1	0 0 0

- Error correction



$\underline{y} = \underline{x} \oplus \underline{z}$

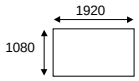
$e \le \left\lfloor \frac{d_{min} - 1}{2} \right\rfloor$ for correcting

2 HDTV – "GRAND ALLIANCE"

Why?

- Digital System Design Example
- Requires algorithms in hardware
- Project tie-ins

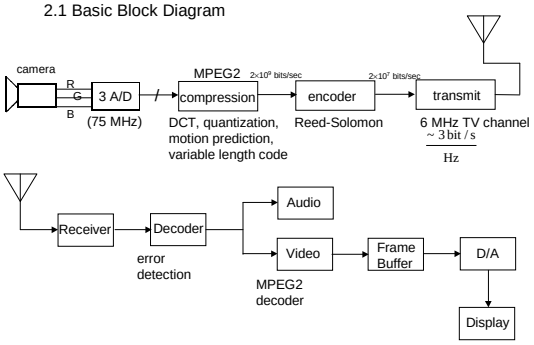
What does it do?



$\times$ 30 frames/sec = 62.2 M pixels/sec @ 10 bits RGB $\approx 2 \times 10^9$ bits/sec

2 HDTV – "GRAND ALLIANCE"

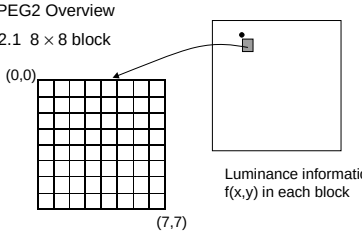
2.1 Basic Block Diagram



2 HDTV – "GRAND ALLIANCE" (cont.)

2.2 MPEG2 Overview

2.2.1 8×8 block



2.2.2 Discrete Cosine Transform

$$DCT: F(u,v) = \sum_i \sum_j d(i,j) \cos\frac{(2u+1)i\pi}{2N} \cos\frac{(2v+1)j\pi}{2N} f(i,j)$$

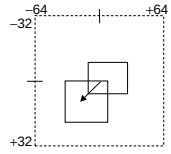
Look at frequency content: high frequency noise, (ignore)

Quantize: 64×8 bits $= 512$ bits $\rightarrow$ 64 b (8 : 1 reduction)

2 HDTV – "GRAND ALLIANCE" (cont.)

2.2 MPEG2 Overview (cont.)

2.2.3 Motion estimation



don't transmit static information

displaced frame difference

Bidirectional motion compensation
I: isolation
P: forward motion compensation
B: bidirectional

Example with variable length code
00000 → 0
0 → 10
1 → 11
00000 1 00000 0 12
→ 0 11 0 0 6

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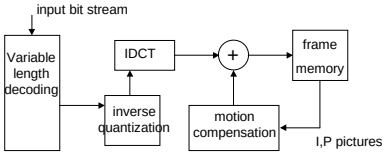
2 HDTV – "GRAND ALLIANCE" (cont.)

2.3 MPEG Video Decoding

Block diagram



Estimate 4 to 5×10^9 IPS

Data transfer rate = 500 Mbytes/sec

Sorry Pentium Pro!

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3 IDCT IN HARDWARE

(Masaki et al.)

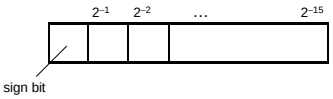
Separable – Use two 1D IDCT

8 pt IDCT

$$x(i) = \sum_{k=0}^{7} c(k)X(k)\cos\frac{(2i+1)k\pi}{16} = \sum_{k=0}^{7} a_K X(k)$$

$$-1 < a_K < 1, \quad -1 < X(k) < 1$$

16 bit two's complement



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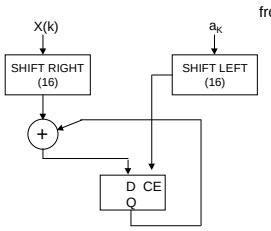
3 IDCT IN HARDWARE (cont.)

3.1 Serial multiplier, 16 clock cycles



from ROM

Unsigned 4 bit example

X(k) = .1001

a_K = .0111

	Shift right	Shift left
total =	.00100	1110
	+ 0010	1100
	+ 0001	1000
	.00111	

roundoff

$$\frac{9}{16}\cdot\frac{7}{16} = \frac{63}{256} \approx \frac{7}{32}$$

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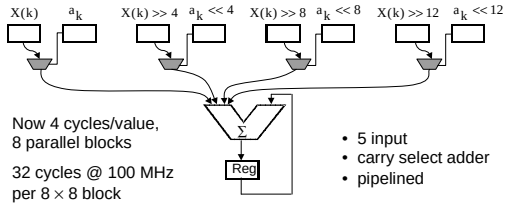
3 IDCT IN HARDWARE (cont.)

Parallelize



Now 4 cycles/value,
8 parallel blocks

32 cycles @ 100 MHz
per 8 × 8 block

- 5 input
- carry select adder
- pipelined

1D IDCT in 0.6µm CMOS

126K transistors, 102 MHz, 360 µW

whole chip 22 mm² (< $10 in high volume)

total 339K transistors, 1.26 W vs. ~10 Pentium @ 10 W each

lower power, lower cost, faster than general purpose CPU