0 Admin
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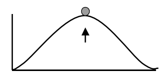
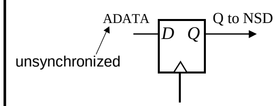
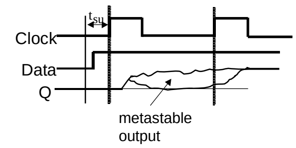
1 RECAP

Metastability – What is it; why is it a problem?

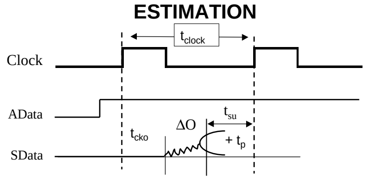






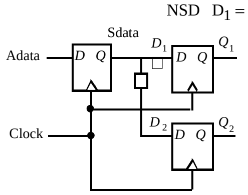
Problem? Causes FSM failure

2 METASTABILITY CONCLUSION – FAILURE RATE ESTIMATION



Trivial state machine

NSD $D_1 = D_2 = SDATA$



Failure: How often is $Q_1 \neq Q_2$?

2 METASTABILITY CONCLUSION – FAILURE RATE ESTIMATION (cont.)

FSM works correctly if ?

$$t_{clock} > ? \quad t_{cko} + \Delta O + t_{su} + t_p$$

Xilinx XC3020-70 family

t_{su} = 5 ns
t_{cko} = 6 ns
$t_p \approx$ 10 ns

If no metastability, $t_{clockmin}$ = 21 ns

$$\text{Failure Rate} = \frac{1}{MTBF} = f_1 \cdot f_2 \cdot k_1 \cdot e^{-k_2 \Delta O}$$

MTBF = mean time between failures
f_1 = clock rate
f_2 = data rate
$k_2 = 3.7 \times 10^9$/sec
$k_1 = 1.5 \times 10^{-10}$ sec

2 METASTABILITY CONCLUSION – FAILURE RATE ESTIMATION (cont.)

Allow 2 ns max for ΔO

$$t_{clock} = 23\,\text{ns} \qquad (43.5\text{MHz})$$

Assume input data rate = 1 MHz
What happens if ΔO > 2 ns?
⇒ setup violation
inconsistent clocking

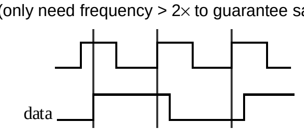
$$\text{Failure rate} = (43.5\text{MHz})(1\text{MHz})(1.5\times10^{-10}\text{ sec})\, e^{-(2.0\times10^{-9})(3.69\times10^{9})}$$
$$= (6.5\times10^{3})e^{-7.38} = 4 \text{ failures/second!}$$

2 METASTABILITY CONCLUSION (cont.)

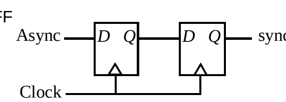
Minimizing Metastability

1. Use good synchronizers (Xilinx FF IFD is good)
2. Slow down clocks – more time to settle

   (only need frequency > 2× to guarantee sample)



3. Extra sync FF



may be important for ATMs, etc.

3 TESTABILITY

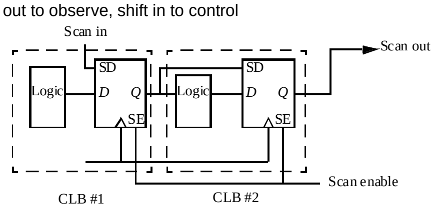
Verify circuit actually works … ship functioning product

Design for testability

$\rightarrow$ controllability – force value of any node
observability – determine value of any node

3.1 Xilinx Boundary Scan Method

Turn all storage elements into giant shift register: Shift out to observe, shift in to control



reading/setting state of two CLBs (technique used by Xchecker)

3 TESTABILITY (cont.)

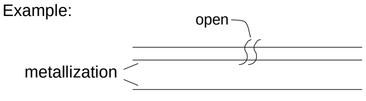
3.1 Xilinx Boundary Scan Method (cont.)

Error sources:

Design errors – logic, timing, self starting, self resetting (caught by sim if models are correct)

Process errors – lower gain, too much resistance, shorts, opens $\rightarrow$ verify that built to design

Example:



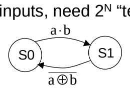
3 TESTABILITY (cont.)

3.2 Exhaustive Testing

Combinational circuit – N inputs, need 2^N "test vectors"

Sequential circuit

Number of vectors?



From every state, 2^N tests total (2^N)(# of states)

computer in class $\rightarrow$ 6 16-bit Reg + 5-bit μPC = 101 bits

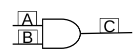
2^{101} states $\approx 2.5 \times 10^{30}$ tests

Pattern sensitivity hard to find

3 TESTABILITY (cont.)

3.3 Stuck at 1, stuck at 0 tests

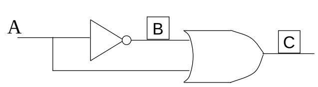
Test AND Gate Model: Single fault



Node	Test vector A B	Expected output
C Sa 0	1 1	1
C Sa 1	00, 01, or 10	0
A Sa 0	1 1	1
A Sa 1	0 1	0
B Sa 0	1 1	1
B Sa 1	1 0	0

3 TESTABILITY (cont.)

Unminimized logic is not testable!



Node	Test vector	If working, expected output
A Sa 0		1
A Sa 1		
B Sa 0 ✓	0	1
B Sa 1		

Can only check 1 node condition!