0 Admin
1 Recap
2 Hierarchical FSM – Timing
3 Metastability – Video

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1 RECAP

Equivalent states:

1) ∀ input combinations, outputs are the same
2) ∀ input combinations, go to equivalent next state

Implication Chart Method:

Step 1: Check that outputs are the same

Step 2: List next states $\boxed{\begin{matrix} S_1 - S_0 \\ S_2 - S_1 \end{matrix}}$

Step 3: Check next states outputs

Step 4: Find equal states

Repeat until all equivalencies are found

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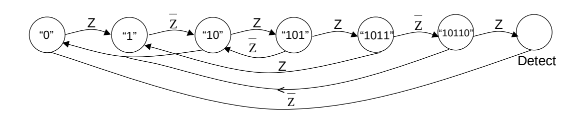
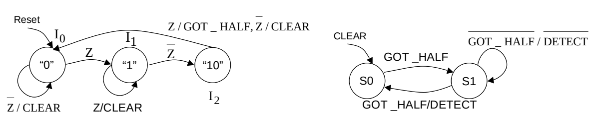
2 HIERARCHICAL FSM EXAMPLE

"101101" detector





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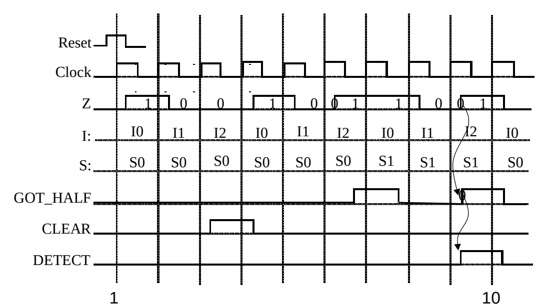
2 HIERARCHICAL FSM EXAMPLE (cont.)

Check with timing diagram Z = 100101101



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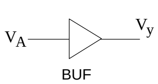
3 METASTABILITY

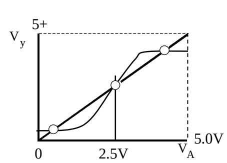
What is it? Where is it from? How bad is it? What can be done about it?

3.1 What is it?

"metastability" = "in between"

Consider analog behavior of a buffer





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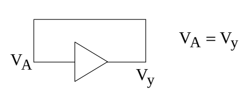
3 METASTABILITY (cont.)

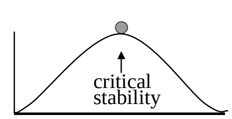
Buffer as latch



$V_A = V_y$

3 points: $\begin{cases} V_A \approx 0.3 = V_y \\ \text{logic } 0 \\ V_A \approx 4.5 \approx V_y \\ \text{logic } 1 \end{cases}$

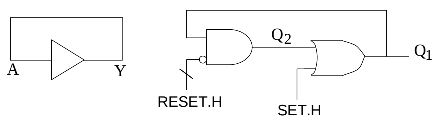
$V_a \approx 2.5 \approx V_y$
metastable



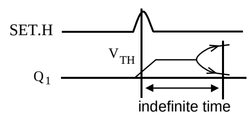
3 METASTABILITY (cont.)

3.2 Where does it come from?

How to get into metastable condition using digital inputs?

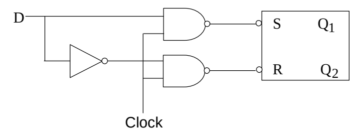


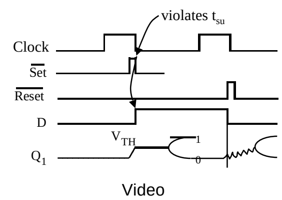
“runt” pulse into latch



3 METASTABILITY (cont.)

Consider D latch

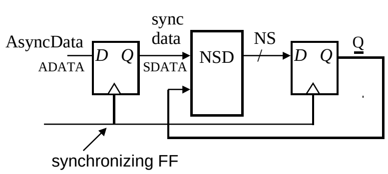




3 METASTABILITY (cont.)

3.3 Why is metastability important?

What can metastable input do to FSM?

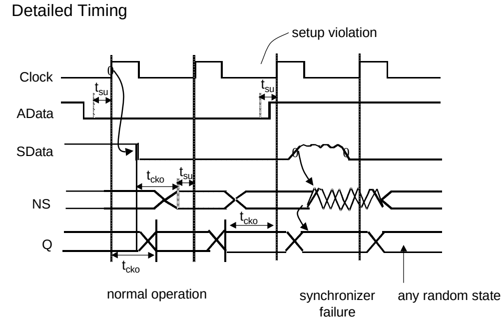


Recall: What happens if no sync FF?

→ random next state

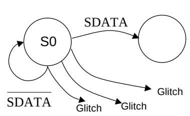
3 METASTABILITY (cont.)

Detailed Timing



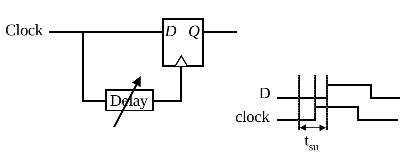
3 METASTABILITY (cont.)

Example



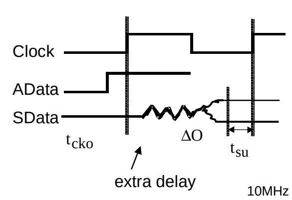
Glitches in NSD? Next state may be indeterminate!

<u>Demo</u>



3 METASTABILITY (cont.)

How bad is it? Maximum duration of metastability ...



10MHz clock
1MHz data
1ns extra delay every 27 ms

No failures longer than 35 ns.