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0 Admin
1 Recap
2 State diagram for simple CPU
3 N-way branch controller
4 2-way branch controller

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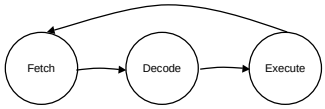
## 1 RECAP




LOAD
STORE
ADD
BRN

Fetch (RTN)
PC→MAR, PC+1→PC
RAM[MAR] →IR

Fetch micro-operations
PC→ABUS, ABUS→MAR, PC+1→PC
(MAR→RAM _ADR, RAM→DATABUS, DATABUS→MBR, MBR→IR)

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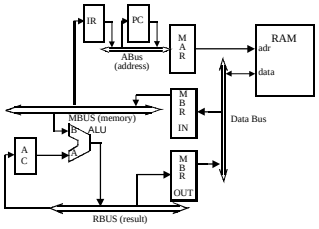
## 1 RECAP (cont.)

Simple CPU data path

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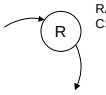
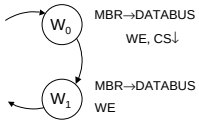
## 1 RECAP (cont.)

Read cycle



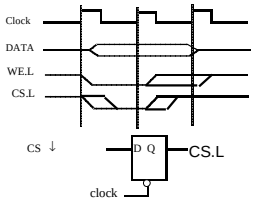

RAM → DATABUS
CS, DATABUS→MBR

Write cycle




MBR→DATABUS
WE, CS↓

MBR→DATABUS
WE

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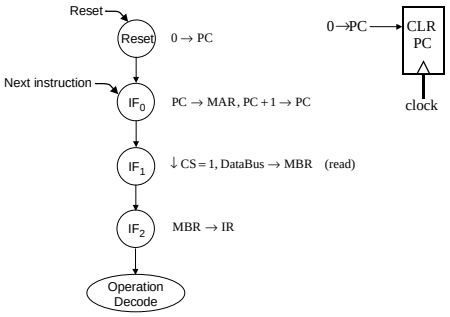
## 2 CONTROLLER STATE DIAGRAM (MOORE MACHINE)

2.1 Fetch

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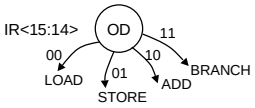
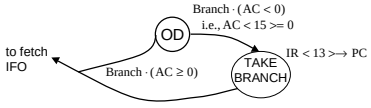
## 2 CONTROLLER STATE DIAGRAM (cont.)

2.2 Decode




2.3 Branch



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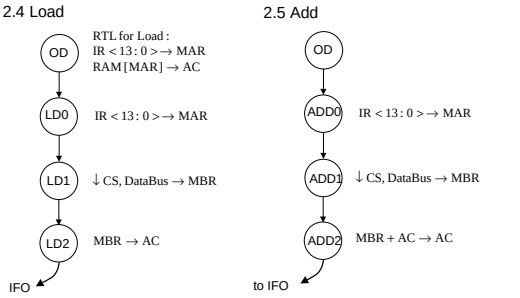
## 2 CONTROLLER STATE DIAGRAM (cont.)

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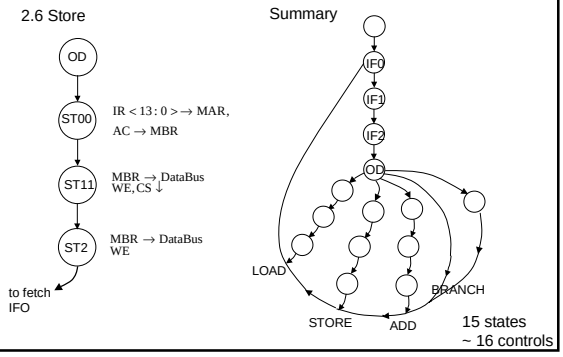
## 2 CONTROLLER STATE DIAGRAM (cont.)

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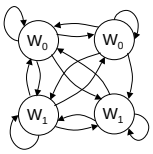
## 3 N-WAY BRANCH CONTROLLER/ROM BASED FSM

"Micro-instruction" – How to make CPU controller

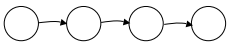
Motivation: State machines are complex




Do we really need so many branches?

CPU State Diagram: Many linear chains

What sequential component has linear chain of states?



? Counter!

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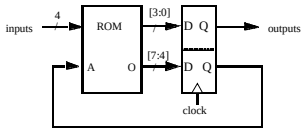
## 3 N-WAY BRANCH CONTROLLER (cont.)

3.1 ROM based FSM (e.g., $256 \times 8$)

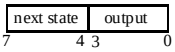



How many inputs? … 4. How many outputs? … 4. States? … 16

Possible state machines? … $16^{16} = 2^{64} = 2 \times 10^{18}$

may be more than we need!

"μ instruction" format




16 possible branches, 4 outputs, 4 inputs

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## 4 2-WAY BRANCH CONTROLLER

Concept: Combine counter and ROM

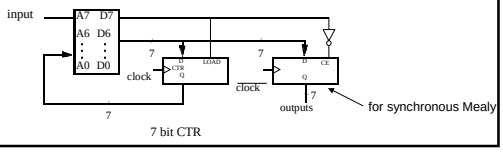
Either:

count and output

or:

branch and no output

Why? More states and more outputs in same ROM size! (fewer inputs)

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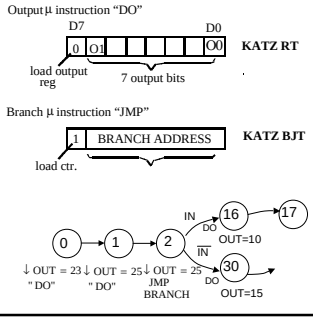
## 4 2-WAY BRANCH CONTROLLER (cont.)

"Instruction" Format – $2^{128}$ "μ programs"

128 "states" (not counting outputs)