0 Admin
1 Recap
2 RTL for instructions/micro-operation
3 Memory interface
4 State diagram for controller

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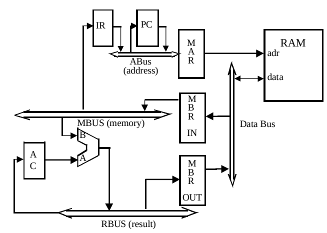
1 RECAP

Simple CPU data path



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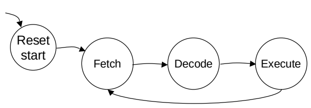
2 INSTRUCTION DESCRIPTION RTL

Registers		
PC	Program counter	Pointer to instruction
IR	Instruction register	Holds current instruction
AC	Accumulator	Data register
MAR	Memory address register	
MBR	Memory bus register	



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2 INSTRUCTION DESCRIPTION RTL (cont.)

2.1 Instruction Fetch

$$\left.\begin{array}{l} PC \rightarrow MAR,\ PC+1 \rightarrow PC \\ RAM[MAR] \rightarrow MBR \\ MBR \rightarrow IR \end{array}\right\} \text{High-level description}$$

2.2 Load XXX memory [XXX] $\rightarrow$ AC

$IR\langle 13{:}0\rangle \rightarrow MAR$
$RAM[MAR] \rightarrow MBR$; read cycle
$MBR \rightarrow AC$

	15	14	
IR:	0	0	XXX

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2 INSTRUCTION DESCRIPTION RTL (cont.)

2.3 Store AC $\rightarrow$ memory [XXX]

$$\left.\begin{array}{l} AC \rightarrow MBR \\ IR\langle 13{:}0\rangle \rightarrow MAR \end{array}\right\}$$
$MBR \rightarrow RAM[MAR]$ write cycle

2.4 Add AC + memory [XXX] $\rightarrow$AC

$IR\langle 13{:}0\rangle \rightarrow MAR$
$RAM[MAR] \rightarrow MBR$
$MBR+AC \rightarrow AC$

2.5 BRN

If A < 0 IR<13:0> $\rightarrow$ PC, else NOP

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2 INSTRUCTION DESCRIPTION RTL (cont.)

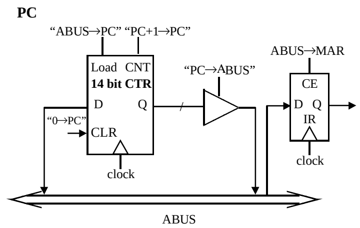
2.6 “Micro-operations”

$PC \rightarrow MAR$	$PC \rightarrow ABUS$, $ABUS \rightarrow MAR$
$MBR \rightarrow IR$	$MBR \rightarrow MBUS$, $MBUS \rightarrow IR$
$IR \rightarrow MAR$	$IR \rightarrow ABUS$, $ABUS \rightarrow MAR$
$MBR \rightarrow AC$	$MBR \rightarrow MBUS$, $MBUS \rightarrow ALUB$, $ALUB \rightarrow RBUS$, $ABUS \rightarrow AC$
$MBR + AC \rightarrow AC$	$MBR \rightarrow MBUS$, $AC + MBUS \rightarrow RBUS \rightarrow AC$
$PC + 1 \rightarrow PC$	$PC + 1 \rightarrow PC$

2.7 Micro-operation Detail (review)

2 INSTRUCTION DESCRIPTION RTL (cont.)

2.7 Micro-operation Detail (review)



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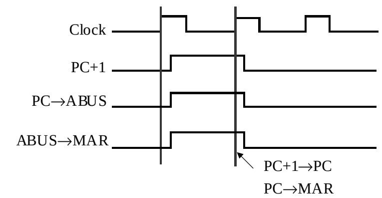
2 INSTRUCTION DESCRIPTION RTL (cont.)

Block Timing: Fetch



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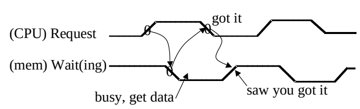
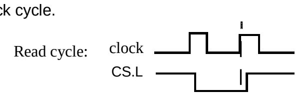
3 MEMORY INTERFACE

Full handshaking (allows variable speed memory)



Fixed speed memory: Simpler, faster if RAM faster than clock cycle.



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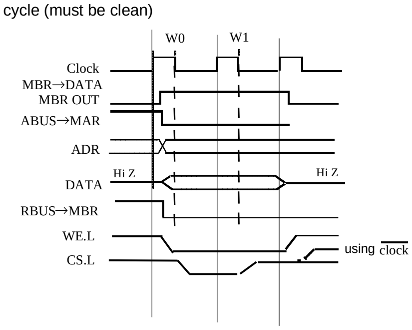
3 MEMORY INTERFACE (cont.)

Write cycle (must be clean)



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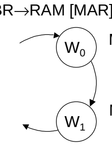
3 MEMORY INTERFACE (cont.)

MBR→RAM [MAR]

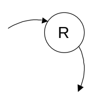


MBR→DATABUS

WE↓, CS↓ must be glitch free

MBR→DATABUS

Read cycle



CS = 1, DATABUS→MBR

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4 STATE DIAGRAM FOR CONTROLLER

Moore Machine