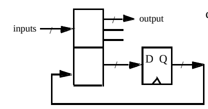
0 Admin
1 Recap
2 Video signals and timing
3 Converting analog voltage to digital values

1 RECAP

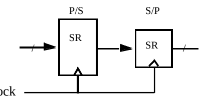
- ROM-based FSM



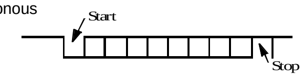
combine OD and NSD

Mealy or Moore? Either!

- Serial transmission – Synchronous



- Serial transmission – Asynchronous

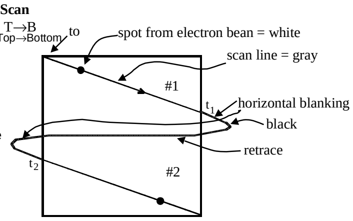


2 VIDEO SIGNALS AND TIMING

Raster Scan

L→R T→B

Left→Right Top→Bottom



Illusion of continuous image due to: 1 persistence of retina

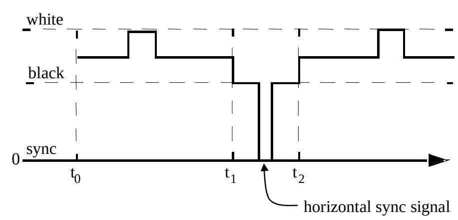
2 persistence of phosphor

Position of dot on screen determined solely by timing – serial data with synchronized signals. Not sent as I(t,y), but I(t).

2 VIDEO SIGNALS AND TIMING (cont.)

Video is an **analog** signal.

Composite sync ÷ video (image data) + synch on same wire



2 VIDEO SIGNALS AND TIMING (cont.)

2.1 TV Camera

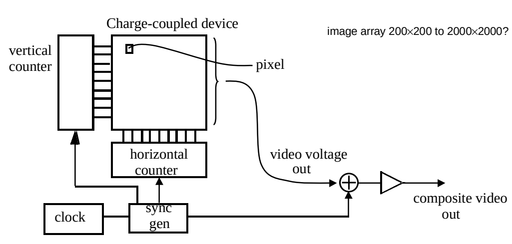


image array 200×200 to 2000×2000?

with high BW amp, might see individual pixels – usually blurred

New cameras: built in A/D converter → direct digital output

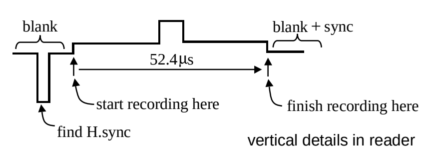
2 VIDEO SIGNALS AND TIMING (cont.)

2.2 Timing and Interface

Problems: 1. Need to convert analog voltage to digital values (A/D)

2. Only care about image data, not blank and sync
⇒ need to ignore blank and sync

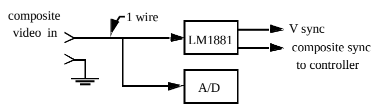
Basic idea – For each line:



vertical details in reader

2 VIDEO SIGNALS AND TIMING (cont.)

LM1881 Sync Detector



Assume V sync and Composite sync are:

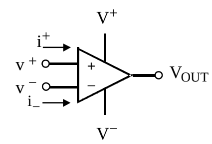
1. glitch free
2. valid logic levels

Anything else to be careful about? (with vsync and csync?) Hint: clocks in camera and FSM?

☞ Asynchronous input! **Must** synchronize → use INFF

3 CONVERTING ANALOG VOLTAGE TO DIGITAL VALUES

3.1 Review ideal op-amp



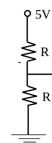
Assumptions:

$V_{out} = A(v^{+} - v^{-})$

$i_{+}, i_{-} = 0$

$V^{-} < V_{out} < V^{+}$

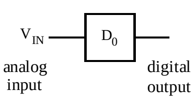
3.2 Review voltage divider



$V_1 = \frac{R}{R+R}(5V) = 2.5V$

3 CONVERTING ANALOG VOLTAGE TO DIGITAL VALUES (cont.)

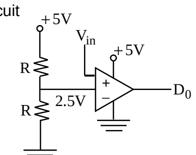
3.3 Design a one-bit analog-to-digital converter with input range $0 < V_{in} < 5V$



$D_0 = \begin{cases} 0 & 0 \le V_{in} < 2.5V \\ 1 & 2.5 \le V_{in} < 5V \end{cases}$

Solution: use op amp and voltage divider

Circuit



check V_{in} < 2.5V

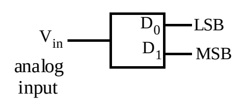
$D_0 = A \quad (V_{in} - 2.5V)$

$= A \quad$ (negative number)

for $A \to \infty, D_0 = 0V$

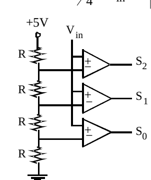
3 CONVERTING ANALOG VOLTAGE TO DIGITAL VALUES (cont.)

3.4 Design two-bit analog converter, input range 5V ("flash" design. Sequential designs also available)



V_{in}	D_1	D_0	S_2	S_1	S_0
$< 5/4$	0	0	0	0	0
$5/4 \le V_{in} \le 5/2$	0	1	0	0	1
$5/2 \le V_{in} \le 15/4$	1	0	0	1	1
$15/4 \le V_{in}$	1	1	1	1	1

How to get 5/4, 5/2, 15/4?



3 CONVERTING ANALOG VOLTAGE TO DIGITAL VALUES (cont.)

Design combinatorial logic to convert S_0, S_1, S_2 to D_1, D_0

Need max. circuit

$D_0 = \overline{S}_2 \overline{S}_1 \cdot S_0 + S_2 \cdot S_1 \cdot S_0$

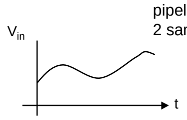
$= S_0 \cdot (S_2 \odot S_1)$

$D_1 = S_1$

3.5 Timing – When is output valid?

pipeline – delay

2 samples delay – your A/D 3 samples



need clock

need to keep input constant while comp. settles

3 CONVERTING ANALOG VOLTAGE TO DIGITAL VALUES (cont.)

3.5 Timing (cont.)