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0 Admin
1 Recap
2 Termination/reflections
3 Decoder
4 ROM
5 RAM

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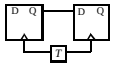
1 RECAP

Timing-related "gotchas"

- Clock skew
  Problem: ? Hold time violation
  Fix: ? BUFGS Low latency clock distribution



- Unsynchronized inputs
  Problem(s): ? Violate setup/hold time ⇒ incorrect FSM operation
  Solution: Synchronize inputs with INFF
- "Long wires" (length > (1/4 rise time) · 0.2 m/ns)
  Problem: Reflections, look-like glitches
  Solution: Termination

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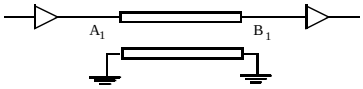
1 RECAP (cont.)

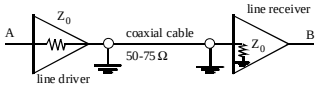
Termination/reflections

Z_0: characteristic impedance
Z_L: load impedance
Z_S: source impedance



$$\Gamma_{B_1} = \frac{Z_L - Z_0}{Z_L + Z_0} \qquad \Gamma_{A_1} = \frac{Z_S - Z_0}{Z_S + Z_0}$$

Impedance matching and termination



$\Gamma_A = \Gamma_B = 0$

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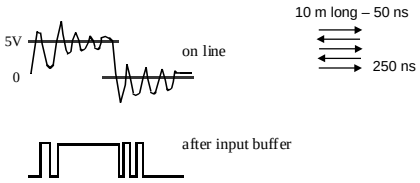
1 RECAP (cont.)

What if impedance in not matched? – May have to wait → multiple reflections

Example: PC printer cable



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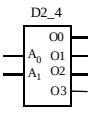
2 DECODER



Truth table

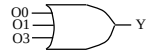
A1	A0	O0	O1	O2	O3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

Use: Can make any Boolean function of A0,A1 using D2-4 and OR gate or select one of 4

Example:

A1	A0	Y
0	0	1
0	1	1
1	0	0
1	1	1

$Y = O0 + O1 + O3$



bigger win for 3 or 4 inputs

efficient for CLBs and debug

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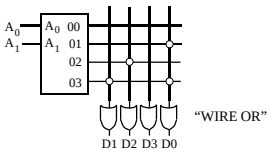
3 READ ONLY MEMORY (ROM)

4 words + 4 bits



A1	A0	D3	D2	D1	D0
0	0	0	0	0	0
0	1	0	0	0	1
1	0	0	1	0	0
1	1	1	0	0	1

anything you want here
$D = A^2$

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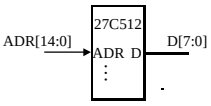
3 READ ONLY MEMORY (cont.)

In Xilinx, each CLB = 32×1 ROM

- 32 CLBs gives 128×8 ROM
- any 8 bit function of 7 bits, e.g., sine, cosine, etc.
- very fast and compact

bigger look up tables? – 27C512 : $32K \times 8$



8 logic functions of 15 variables, or, e.g.,

$$D = \sqrt{ADR[14:7]^2 + ADR[6:0]^2}$$

$$= X[7:0]^2 + Y^2[6:0]$$

also great for NSD

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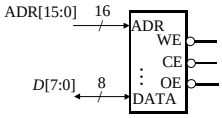
4 RANDOM ACCESS MEMORY (RAM)

read write memory – large quantity of temporary storage

Lab 7 RS5128 : $64K \times 8$ bits (internal $256 \times 256 \times 8$)

Note: data is bi-directional input and output $\rightarrow$ tri-stated



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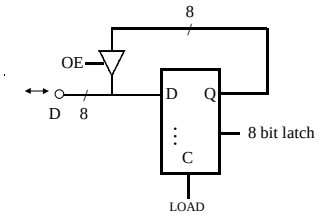
4 RAM (cont.)

4.1 Conceptual Building Blocks – Internal organization

Internal level sensitive latch



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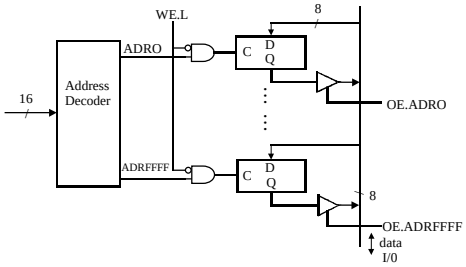
4 RAM (cont.)

4.1 Conceptual Building Blocks (cont.)

Selecting 1 of 2^{16} latches



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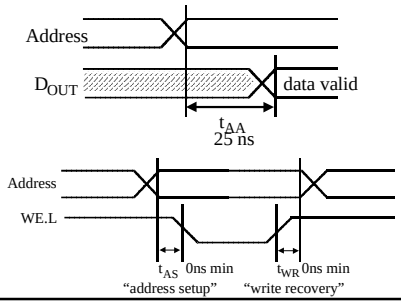
4 RAM (cont.)

4.2 RAM Timing – Read and Write Cycles

READ cycle: Assume CEIB = L, CE2 = H, OEB = L



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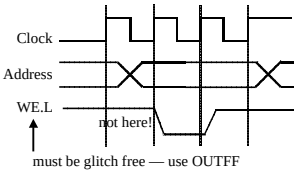
4 RAM (cont.)

4.2 RAM Timing (cont.)

How to corrupt memory? – skew or glitch on WE line

WE = clock of level sensitive

How to be safe?