University of California at Berkeley
College of Engineering
Department of Electrical Engineering and Computer Sciences

CS150
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Checkpoint 2
Video Interface

1. Objective

For this checkpoint, you will

1. Wire-up the Video Sync Separator and A/D Converter
2. Build the video interface

2. Introduction

The video signal generated by the camera is a composite video signal. In this checkpoint, you'll use LM1881 Sync Separator and HI1175 Analog to Digital converter to build the video interface. The LM1881 Video Sync Separator will help you to find out where the top and left side for the image is, and the HI1175 A/D converter will converts the analog data from the video camera into 8 bits of digital data, which can be stored into the SARM. Logic analyzer will be used to check off your video interface.

3. Wiring-up of the video interface

3.1 LM1881 Video Sync Separator

The LM1881 video sync separator takes as input the composite video signal, and provides outputs of composite sync and vertical sync, which can be used to find out the beginning of the video frame and the beginning of the line.

3.2 HI1175 A/D Converter

The HI1175 is an 8-bit analog-to-digital converter. Its electrical interface is

- an analog input ***Vin***
- eight digital data outputs ***D0~D7***
- an clock input ***Clk***
- an active low chip enable input $\overline{OE}$
- an reference voltage (top) V_{RT} which gives +2.6V if shorted with V_{RTS}, the internal voltage reference(top)
- an reference voltage(bottom) V_{BT} which gives +0.6V if shorted with V_{BTS}, the internal voltage reference(bottom)
- digital power DV_{dd} and digial ground DV_{ss}
- analog power AV_{dd} and analog ground AV_{ss}

3.3 The Video Buffer and RC Network

We provide the necessary buffer and RC network for your LM1881 video sync separator and HI1175 A/D converter.

Wire up the video interface according to Fig.2. Please note the $\overline{\textbf{OE}}$ signal of the *SRAM* should be wired to **p18** of XILINX, which is different from the LAB7.

4. Testing the video interface

We provide a bit file *Wvlib\cs150\check2.bit* which can test your wiring. However, you need to build your own test circuit for the A/D converter. The top page *Wvlib/cs150/sch/check.1* is provided for your test circuit, which defines the input and output interface of the XILINX. To test the A/D converter, the *OE* should be high to enable the A/D chip, and you also need to generate the clock signal *VCLK* for the A/D converter. The *VCLK* should have the speed that you need for your resolution, i.e. 200, 220, or 240 horizontal. Note that the clock signal *CLK* of your XILINX comes from the oscillator on your board which has a frequency of 16MHz. It is OK if you only get 80% of the image. Show your TA with logic analyzer the *composite sync output* and *vertical sync output* from the LM1881, and the *clock* and *D0~D7* of the A/D converter.

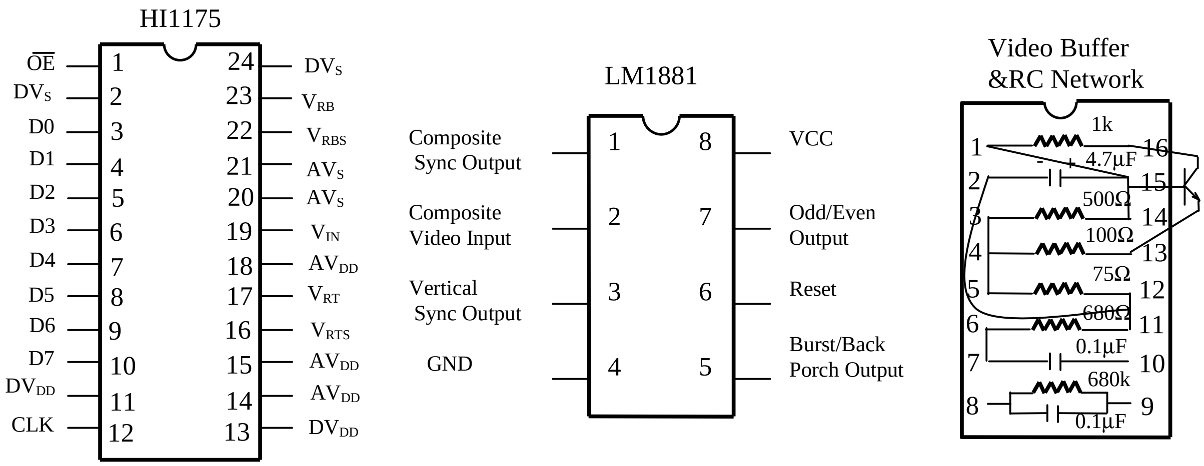

Figure 1 Pinout (top view) of HI1775, LM1881 and Video Buffer&RC Network

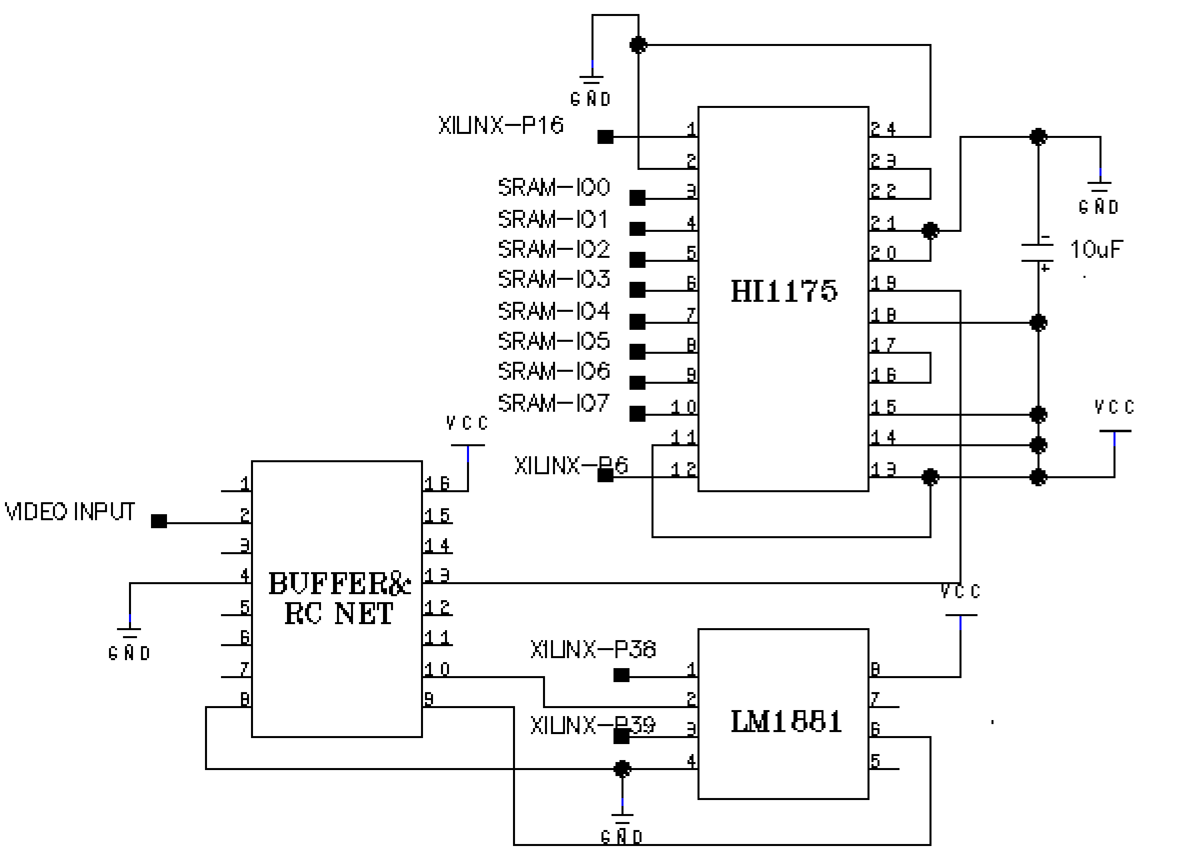

Figure 2 Wiring-up of the video interface
(Note: The pin assignment of **SRAM** is the same as that of the LAB7, *EXCEPT* the ***OE*** signal.
You should connect the ***OE*** of your SRAM to **XILINX-P18**)

Name____ Name____
Lab Section (Check One)
M: ☐ AM ☐ PM T: ☐ AM ☐ PM W: ☐ AM ☐ PM Th: ☐ PM

5. Checkoffs

1. Video Interface wired up (neatly for full credit)
   (Due at the start of the lab session) TA: ____________(30%)

2. Functioning Sync Separator TA: ____________(30%)

3. Functioning A/D Converter TA: ____________(40%)

4. Turned in on time TA: ____________ (100%) (full credit)

5. Turned in one week late TA: ____________ (50%) (half credit)

REMINDER: You need the complete state diagrams for your project for week 2 design review with your TA! See project specification.

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HI1175

DV_{SS}	24	1	$\overline{OE}$
V_{RB}	23	2	DV_{SS}
V_{RBS}	22	3	D0
AV_{SS}	21	4	D1
AV_{SS}	20	5	D2
V_{IN}	19	6	D3
AV_{DD}	18	7	D4
V_{RT}	17	8	D5
V_{RTS}	16	9	D6
AV_{DD}	15	10	D7
AV_{DD}	14	11	DV_{DD}
DV_{DD}	13	12	CLK

HI1175

DV_{SS}	24	1	$\overline{OE}$
V_{RB}	23	2	DV_{SS}
V_{RBS}	22	3	D0
AV_{SS}	21	4	D1
AV_{SS}	20	5	D2
V_{IN}	19	6	D3
AV_{DD}	18	7	D4
V_{RT}	17	8	D5
V_{RTS}	16	9	D6
AV_{DD}	15	10	D7
AV_{DD}	14	11	DV_{DD}
DV_{DD}	13	12	CLK

HI1175

DV_{SS}	24	1	$\overline{OE}$
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AV_{SS}	20	5	D2
V_{IN}	19	6	D3
AV_{DD}	18	7	D4
V_{RT}	17	8	D5
V_{RTS}	16	9	D6
AV_{DD}	15	10	D7
AV_{DD}	14	11	DV_{DD}
DV_{DD}	13	12	CLK