University of California at Berkeley
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EECS150
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Checkpoint 2
Video Interface

1. Objective

In this checkpoint, you will:

1. Wire-up the Video Sync Separator, A/D Converter, video camera, and Op-amp
2. Learn how to manipulate the A/D converter chip

2. Introduction

The video signal generated by the camera is a composite video signal. In this checkpoint, you will use the LM1881 Sync Separator and the HI1175 Analog to Digital converter to build the video interface. The LM1881 Video Sync Separator will help you to find out where the top and left edge of the image is, and the HI1175 A/D converter will convert the analog data from the video camera into 8 bits of digital data. This can be stored into the SRAM. The logic analyzer will be used to check off your video interface.

3. Wiring-up of the video interface

3.1 Video Camera

The video camera used in the project is an NTSC standard camera. It generates an NTSC compatible signal, which was explained in the project specification sheet and is also shown in Figure 1. The camera is connected to the Xilinx board through a 5 pin-DIN connector, which is located near the power plugs. The power of the camera is provided by the Xilinx board, thus you will need to wire up the power lines to the camera from the nearest “+” and “-“ pins. After you finish wiring up the camera connector, you can check if the camera works with an analog channel on the oscilloscope. At the video out pin of the camera, you should see a waveform similar to (a) on Figure 1. For the camera DIN connector pinouts, look at the diagram on the camera housing.

3.2 LM1881 Video Sync Separator

The LM1881 takes the composite video signal as an input, and provides outputs for vertical sync and composite sync, which can be used to find the beginning of a video frame and the beginning of a line respectively. Refer to Figure 1 for the input to the LM1881 and the corresponding outputs - composite sync and vertical sync. For pinouts, refer to Figure 2.

3.3 HI1175 A/D Converter

The HI1175 is an 8-bit analog-to-digital converter. It takes analog input through the Vin pin, and outputs an 8-bit digital output through D0 - D7 pins, which are tri-state buffered by OE.L pin. There is a 2.5 clock cycle delay on the data. On every falling clock edge, the chip samples the analog input and outputs a digital representation on the output pins after a 2.5 clock cycle + 18ns. You should use data on output pins three clock cycles after the sampling, falling edge. Refer to Figure 3 for the timing diagram.
Its electrical interface is:

- an analog input ***Vin***
- eight digital data outputs ***D0~D7***
- a clock input ***Clk***
- an active low output enable input **$\overline{\text{OE.L}}$ –** When OE.L = 0, Data is valid; When OE.L = 1, D0-D7 pins high impedance
- a reference voltage (top) V_{RT} which gives +2.6V if shorted with V_{RTS}, the internal voltage reference(top)
- a reference voltage(bottom) V_{BT} which gives +0.6V if shorted with V_{BTS}, the internal voltage reference(bottom)
- digital power DV_{dd} and digial ground DV_{ss}
- analog power AV_{dd} and analog ground Av_{ss}

For pinouts, refer to Figure 4.

* Since the HI1175 has a different width than the chips that have been used in lab, a pin expander was handed out. When you wire up the A/D converter, don't forget to use it.

3.4 LT1213 Op Amp

The LT1213 is a dual, single-supply, precision op amp. In this checkpoint, only one op amp is used to double the amplitude of the video signal. The op amp is configured in non-inverting mode, and the external circuitry set-up around the op amp, which is provided by RC network, accomplishes the amplification. The benefit of using the op amp as a pre-amp to the A/D converter is an improvement in the resolution per bit. This way, we get a clean, sharp image from the A/D converter. For pinouts, refer to Figure 5.

3.5 RC Network

The RC network provides external miscellaneous circuitry for your LM1881 video sync separator, HI1175 A/D converter, and LT1213 op amp. For pinouts and the schematic of the RC network, refer to Figure 6. Wire up the video interface according to Fig.7

4. Testing the video interface

We provide a bit file *Wvlib\cs150\check2.bit* which can test your wiring. However, you need to build your own test circuit for the A/D converter. The top page *Wvlib/cs150/sch/check.1* is provided for your test circuit, which defines the input and output interface of the XILINX. To test the A/D converter, the *OE* should be high to enable the A/D chip, and you also need to generate the clock signal *VCLK* for the A/D converter. The *VCLK* should have the frequency that you need for your horizontal resolution, i.e. 190, 210, or 230 pixels horizontally. Note that the clock signal *CLK* of your XILINX comes from the oscillator on your board that has a frequency of 16MHz. As noted in the project spec, during one horizontal sync period - 63.5us, the real image signal comes only for 53.3us. Therefore, choose such a VCLK frequency that will allow you to sample a wider image as possible. Also, be careful not to skip a line. You should get at least 80% of the image. Show your TA, with logic analyzer, the *composite sync output* and *vertical sync output* from the LM1881, and the CLK and *D0~D7* of the A/D converter.

Application Notes (Continued)

Figure 1. LM1881 Timing Diagram

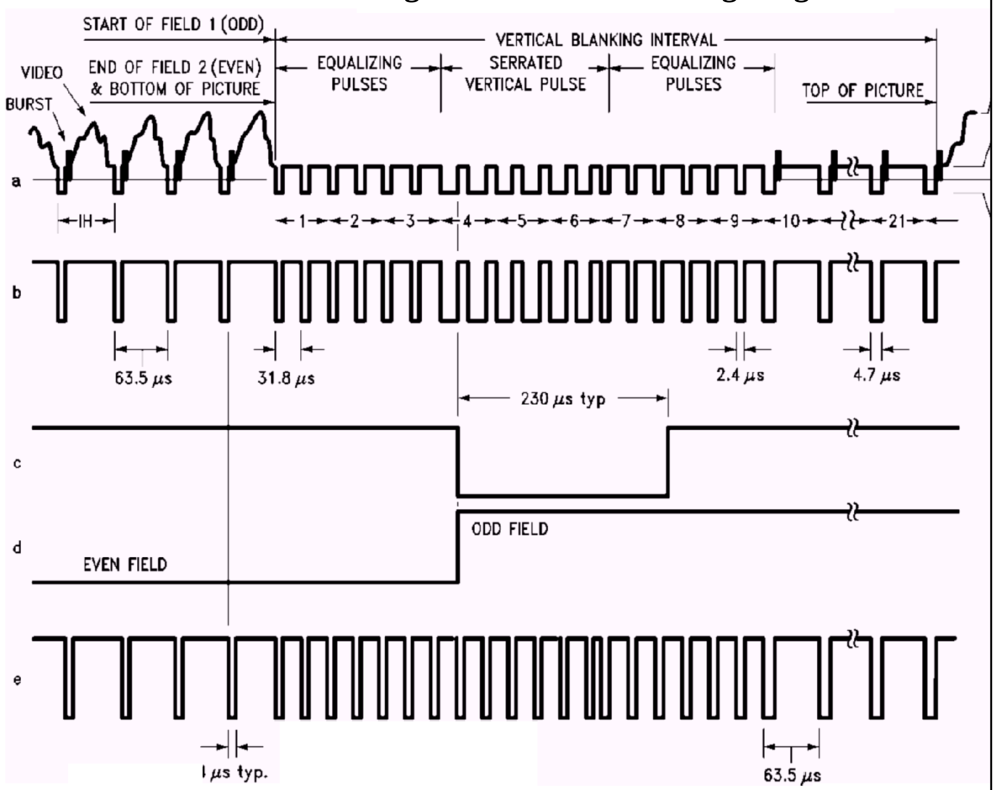
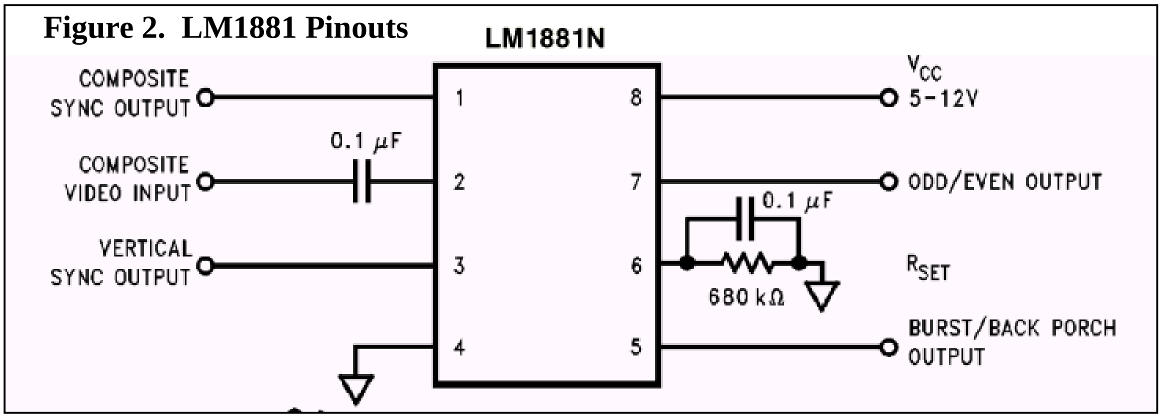


FIGURE 2. (a) Composite Video; (b) Composite Sync; (c) Vertical Output Pulse; (d) Odd/Even Field Index; (e) Burst Gate/Back Porch Clamp

Figure 2. LM1881 Pinouts



Timing Diagrams

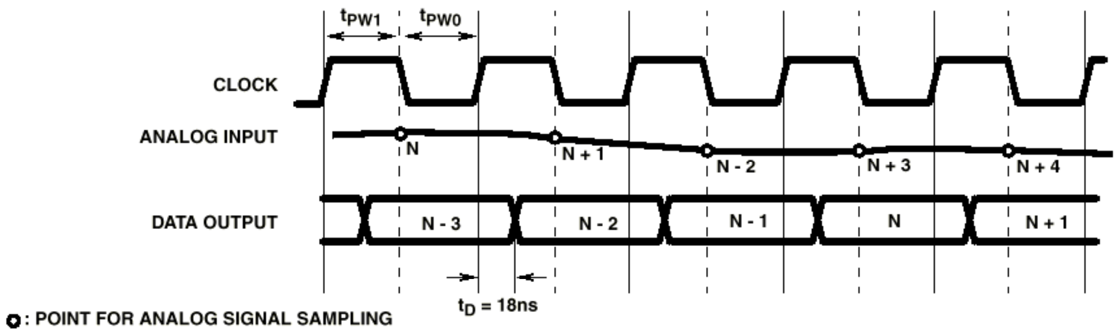


Figure 3. HI1175 Timing Diagram

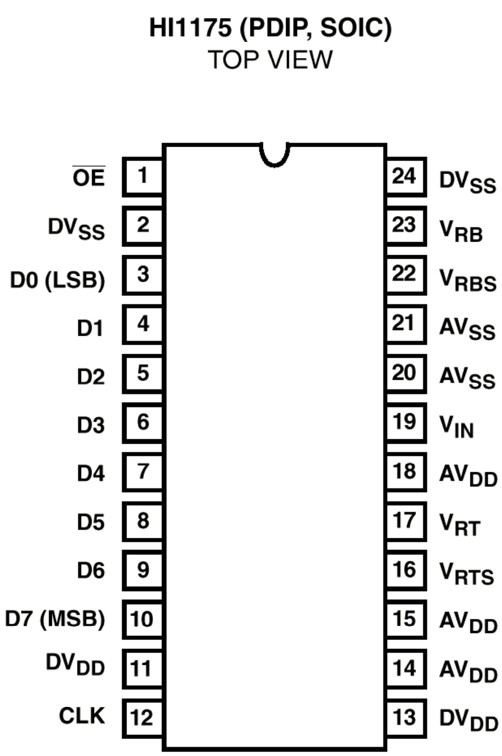


Figure 4. HI1175 Pinouts

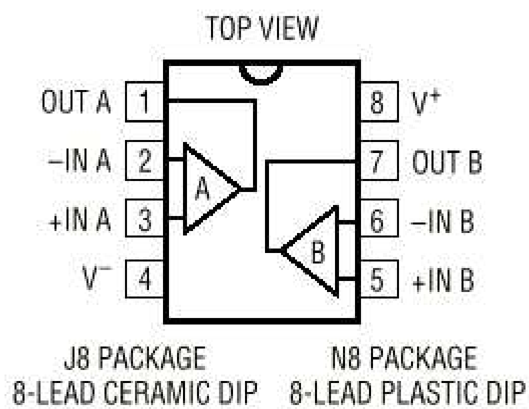


Figure 5. LT1213 Pinouts

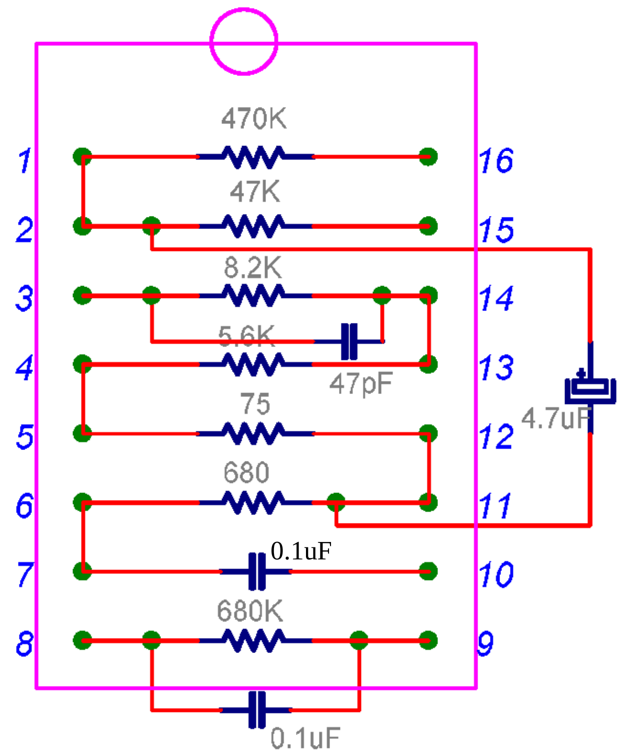


Figure 6. RC Network Pinout and Schematic

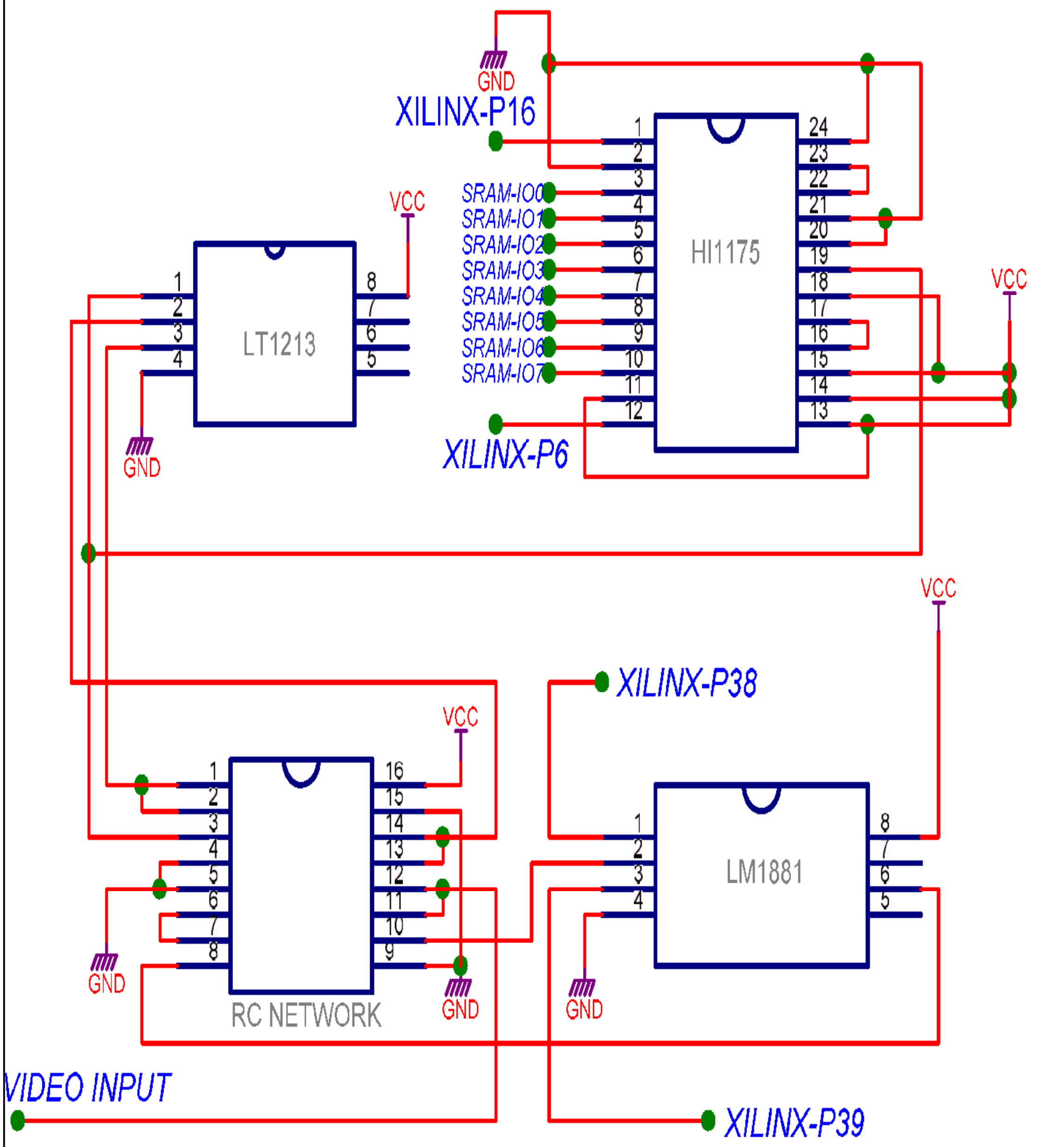


Figure 7. Checkpoint2 Schematic

Name ________________________________ Name________________________________

Lab Section (Check One)

M: __AM __ PM T: __AM __PM W: __AM __PM Th: __PM

5. Checkoffs

1. Video Interface wired up (neatly for full credit)
   (Due at the start of the lab session) TA: ____________(30%)

2. Functioning Sync Separator TA: ____________(30%)

3. Functioning A/D Converter TA: ____________(40%)

4. Turned in on time TA: _________________(100%) (full credit)

5. Turned in one week late TA: ________________ (50%) (half credit)

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HI1175

Dvss	24	1	$\overline{OE}$
VRB	23	2	DVSS
VRBS	22	3	D0(LSB)
AVSS	21	4	D1
AVSS	20	5	D2
VIN	19	6	D3
AVDD	18	7	D4
VRT	17	8	D5
VRTS	16	9	D6
AVDD	15	10	D7(MSB)
AVDD	14	11	DVDD
DVDD	13	12	CLK

LM1881

VCC	8	1	COMP SYNC
O/D	7	2	COMP VIDEO
RSET	6	3	V SYNC
BURST	5	4	GND

LM1881

VCC	8	1	COMP SYNC
O/D	7	2	COMP VIDEO
RSET	6	3	V SYNC
BURST	5	4	GND

LT1213

V+	8	1	OUT A
OUT B	7	2	-IN A
-IN B	6	3	+ IN A
+ IN B	5	4	V-

LT1213

V+	8	1	OUT A
OUT B	7	2	-IN A
-IN B	6	3	+ IN A
+ IN B	5	4	V-

RCN

16	1
15	2
14	3
13	4
12	5
11	6
10	7
9	8