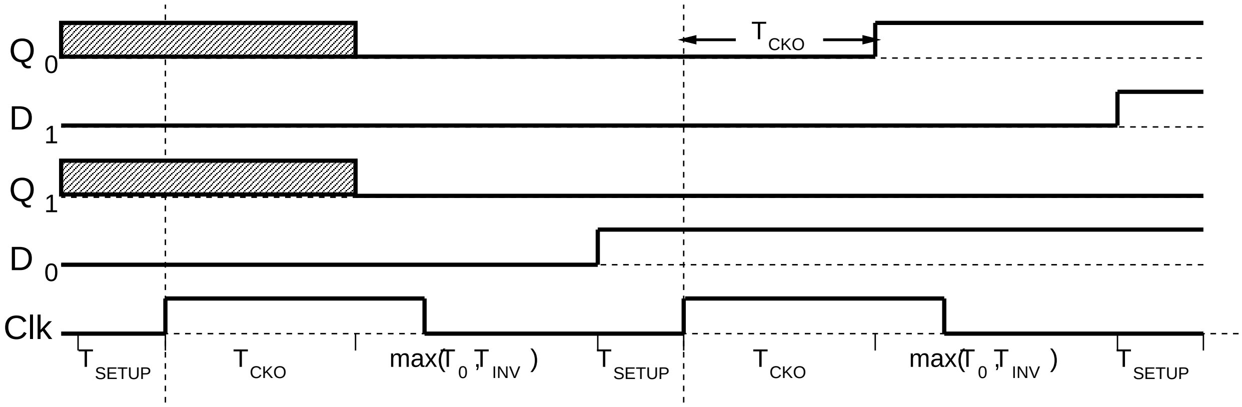
Solution Set 6

gmoy@eecs.berkeley.edu

Problem 1

$T_{SETUP} = 4ns, T_{CKO} < 2.7ns, T_{INV} = 6ns, T_0 = 15ns, T_1 = 75ns, T_2 = 10ns.$

a) Assume that $COUNT$ is always high. This way, we will be looking at the FDREs. Problems with $COUNT$ will be discussed in parts b and c.

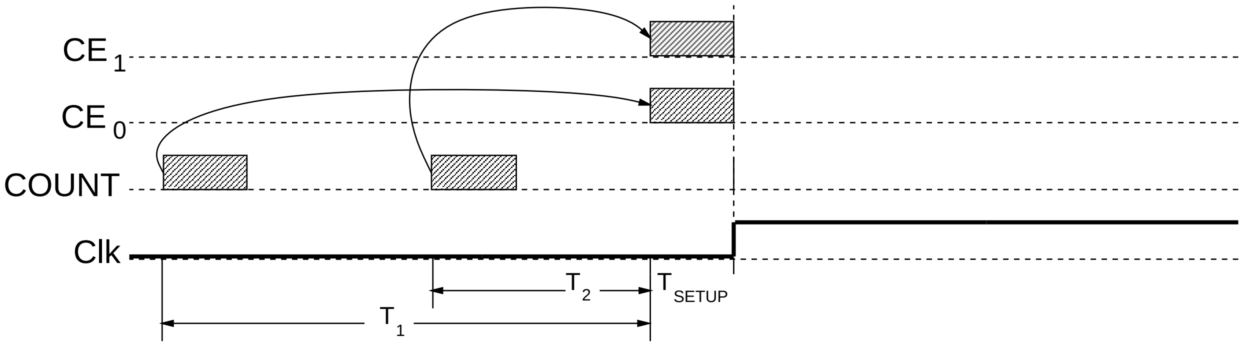


Clock period $= T_{CKO} + max(T_0, T_{INV}) + T_{SETUP} = 3.7ns + 15ns + 4ns = 22.7ns$
Maximum clock frequency $= 44.1MHz$

b) We are looking for the time periods in which a transition of $COUNT$ would violate the setup time of CE_0 and CE_1.

A transition of $COUNT$ between $-(T_1 + T_{SETUP}) < t < -(T_1)$ would cause a setup violation for CE_0. $(-79ns < t < -75ns)$

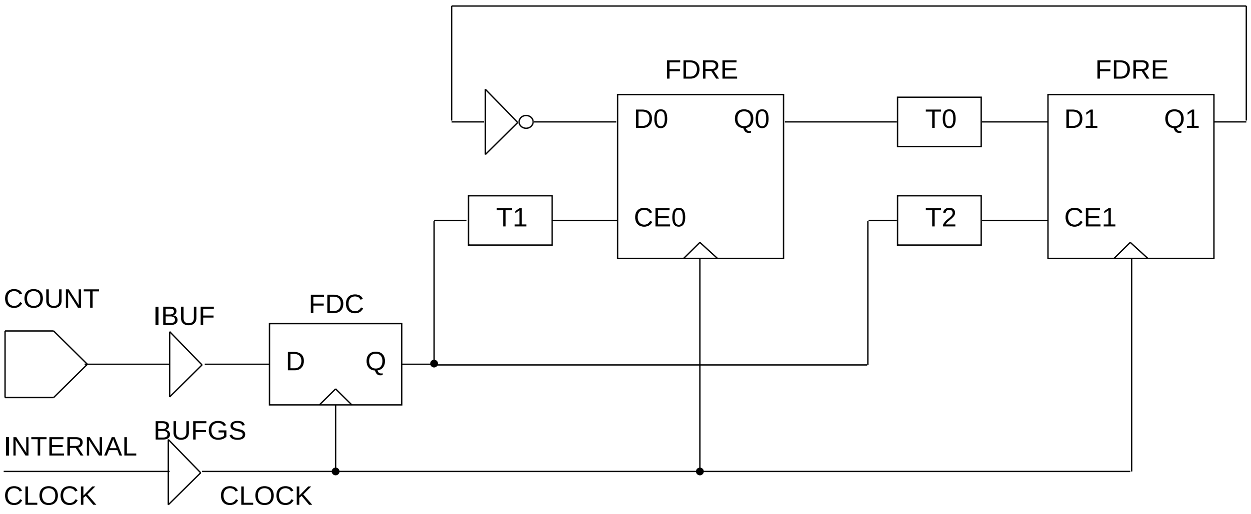
A transition of $COUNT$ between $-(T_2 + T_{SETUP}) < t < -(T_2)$ would cause a setup violation for CE_1. $(-14ns < t < -10ns)$

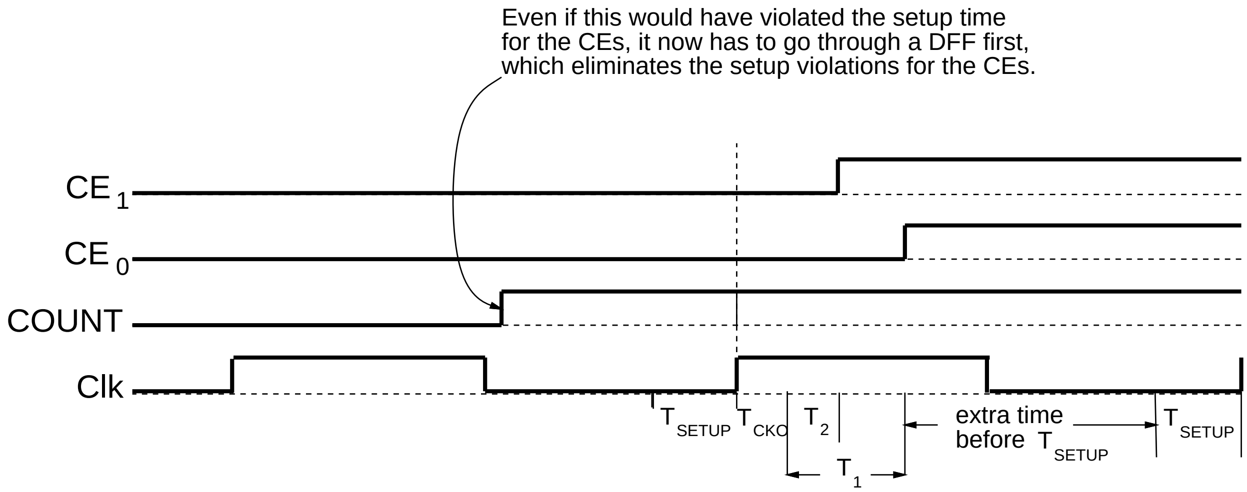


c) Chance of violation = Chance of a transition during setup time. A $2MHz$ clock has a period on $500ns$.

Chance of violation $= \frac{2T_{SETUP}}{1\ period} = \frac{8ns}{500ns} = 1.6\%$

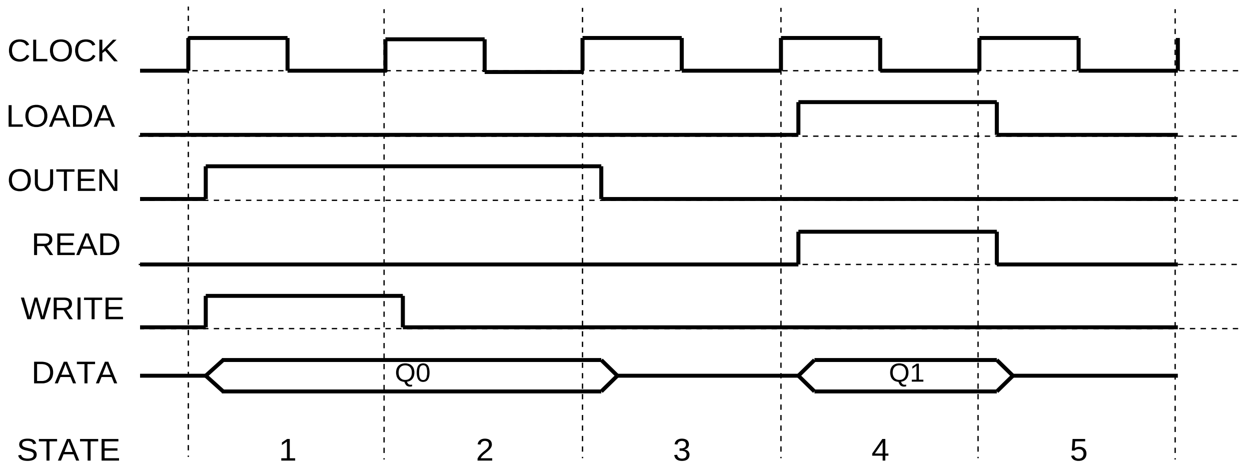
d) To reduce the chance of a randomly occuring $COUNT$ pulse, put an INFF on the $COUNT$ line to make sure changes only occur on the rising edge of the clock. This way, CE_0 and CE_1 will be stable $(T_{PERIOD} - T_{TCKO} - T_{1\ or\ 2})ns$ before the rising clock edge. There exist possible setup violations with the INFF, but we won't worry about that until we talk about metastability in Lecture 23.


FDRE
FDRE
D0
Q0
T0
D1
Q1
T1
CE0
T2
CE1
COUNT
IBUF
FDC
D
Q
INTERNAL
BUFGS
CLOCK
CLOCK


Even if this would have violated the setup time
for the CEs, it now has to go through a DFF first,
which eliminates the setup violations for the CEs.
CE 1
CE 0
COUNT
Clk
T SETUP
T CKO
T 2
T 1
extra time
before T SETUP
T SETUP

Problem 2

a)

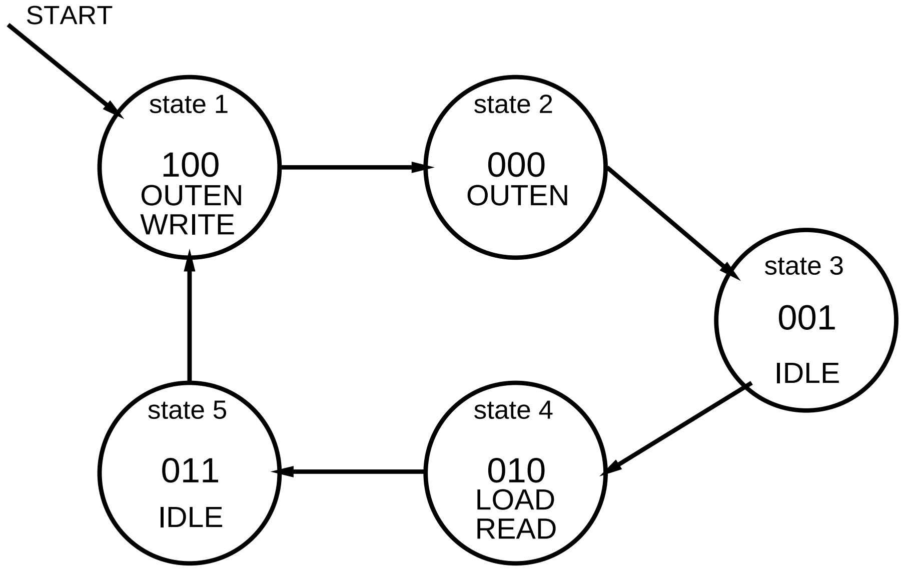

CLOCK
LOADA
OUTEN
READ
WRITE
DATA
Q0
Q1
STATE
1
2
3
4
5

b) Using the CMOS charts:

ILD Pad to I1 via latch	T_{PDLIC}	10.8ns
ODFE global clock to output	T_{ICKOF}	14.0ns
3-state to Pad active + valid, fast	T_{TSONFC}	9.1ns
Setup Time - Pad to Clock	T_{PICKC}	6.0ns
3-state to Pad, hi-Z	T_{TSHZC}	5.2ns
Propagation Delay, Pad to I1, I2	T_{PIDC}	5.5ns
ODFE Setup, Output to Clock	T_{OOK}	5.0ns

In state 1:
 9.1ns delay from setting $OUTEN$ to active, T_{TSONFC}
 6.0ns delay from setup time of $DATA$, T_{PICKC}
 15.1ns total delay ($WRITE$ is done in parallel, and takes T_{PIDC} to set to G of ILD)
In state 2:
 necessary for hold time, also state 2+3 ¿ T_{PDLIC}
In state 3:
 5.2ns delay from setting $OUTEN$ to hi-Z, T_{TSHZC}
In state 4:
 5.5ns delay from propagation delay from Pad to I1 ($READ$), T_{PIDC}
 9.1ns delay from setting $READ$ to active, T_{TSONFC}
 5.5ns delay from propagation delay from Pad to I1 ($DATA$), T_{PIDC}
 5.0ns delay from setup time of $LOADA$, T_{OOK}
 25.1ns total delay
In state 5:
 5.2ns delay from setting $READ$ to hi-Z, T_{TSHZC}
So assuming a constant clock period of 25.1ns, this operation will take 25.1ns x 5 = 125.5ns.

c) You need 5 states to complete this operation. The $WRITE$, $OUTEN$, and $READ$ signals need to be glitch free. To ensure a glitch free signal, it should come from a Flip-Flop.



Use a 3 bit counter with a synchronous reset as the FSM. Use the most significant bit as the WRITE signal.

Use other combinational logic to obtain the other input signals.

Problem 3

There are 32 outputs, 20pF each.

a) $I = C\frac{dV}{dt}$, parallel capacitances add, dV = 5 Volts (or 5.5 Volts is acceptable too since that's what the tables say).

$I = 640pF\frac{5}{dt}$.

Use CMOS charts.
Page 4-106: $T_{OPS} = 12.0ns$, $T_{OPF} = 8.0ns$.
Page 4-106, Footnote 1: For a slow slew rate, the rise times are twice as long as the fast slew rate times. Guess that fast slew rate is approximately $5V/4ns$, and slow slew rate is approximately $5V/8ns$.

Fast:
$\frac{dV}{dt} = 1.25e^9 V/s$, $I = 32 * 20e^{-12} pF * 1.25e^9 V/s = 0.8A$
Slow:
$\frac{dV}{dt} = 0.625e^9 V/s$, $I = 32 * 20e^{-12} pF * 0.625e^9 V/s = 0.4A$

b) Thin wires increase resistance, and long wires increase the transmission line effects, and increase inductance. Resistance $= \rho \frac{L}{A}$ where ρ is the resistivity, L is the length of the wire, and A is the cross sectional area of the wire. There will also be ground bounce due to $V = L\frac{di}{dt}$.