Professor Fearing EECS150/Problem Set 9 Fall 1998

Due at 10 am, Fri. Oct. 30 in box outside 218 Cory Hall

(This problem set may be done individually or by a group of two people maximum. A group of two should hand in a single copy of the solution with both names affixed).

Quiz 2: Tues. Nov. 10 in class.

1. (30 pts)

Katz Chapter 11, problem 3.

2. (40 pts)

Katz Ch 11, problem 7.

3. (30 pts)

a. Show with a timing diagram the operation of the processor during the **ADD** instruction (see problem 2). Show CLOCK and all relevant control signals, and show data bus valid or tri-state times, labelling bus with contents, e.g. "bus=r0", and indicate the clock edge when a particular operation occurs.

b. repeat (3a) but for **RSR** instruction.