Professor Fearing EECS150/Problem Set 8 Fall 1998

Due at 10 am, Fri. Oct. 23 in box outside 218 Cory Hall

(This problem set may be done individually or by a group of two people maximum. A group of two should hand in a single copy of the solution with both names affixed).

1. Xilinx Stuff (15 pts)

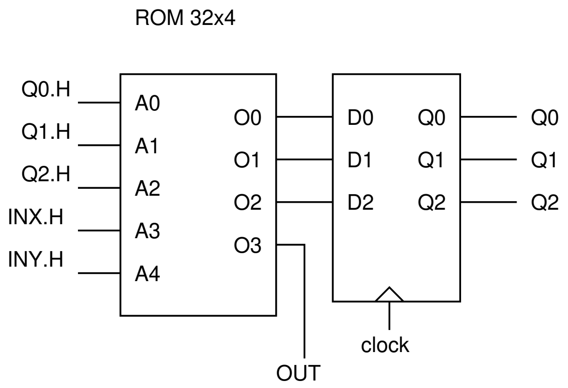
a. What is a UPAD good for? How many are there in an XC4005 in 84 pin package like we are using? List some good uses for these extra flip flops.
b. In what situation might you want to use an IPAD and IFD rather than an IPAD, IBUF, and FD?

2. Successive Approximation Design Example (60 pts)

You are given a black box containing combinational logic which takes an analog input V_{IN} and 8 binary inputs DAC[7:0]. The black box has a single digital output GREATER.H which is asserted if DAC[0:7]/128 (in volts) is greater than V_{IN}. (For example, if $V_{IN} = 1.2499$ volts, then GREATER would be asserted if $DAC > 160_{TEN}$.) Design a digital system, showing block diagram, state diagram, state table, control FSM, and timing diagram, which outputs an 8 bit byte OUT[7:0] and strobe DONE.H as few cycles as possible after a START.H signal is received. (You may assume that V_{IN} is held constant until the DONE signal is asserted.) (Suggestion: do a binary search, starting with MSB. Hint: toggle flip flops.)

3. ROM Based FSM (25 pts)

Using the ROM based FSM shown below, with ROM contents as listed in Table 1, draw a state table and state diagram for the FSM. Explain why this is a Moore or Mealey type FSM. Consider synchronized inputs INX.H and INY.H. INY is asserted before the rising edge of clock cycle 0, then deasserted after the rising edge. Then the following data is presented in order at INX: 1,1,1,0,0,1,1,0,0,1,0. Draw a timing diagram showing CLOCK.H, INX.H, INY.H, and OUT.H.



Adr	Data	Adr	Data	Adr	Data	Adr	Data
0	1	8	0	10	7	18	7
1	2	9	0	11	7	19	7
2	3	A	8	12	7	1A	7
3	4	B	1	13	7	1B	7
4	5	C	2	14	7	1C	7
5	6	D	3	15	7	1D	7
6	7	E	C	16	7	1E	7
7	7	F	6	17	7	1F	7