Professor Fearing EECS150/Problem Set 6 Fall 1998

Due at 10 am, Fri. Oct. 9 in box outside 218 Cory Hall

1. Synchronization (50 pts)

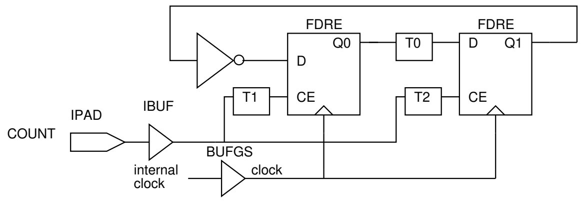
This question illustrates the potential problems caused by feeding asynchronous inputs into a FSM. (Even ignoring metastability). Consider a digital system implemented using a Xilinx 4005E-4 containing a 2 bit binary counter using two FDRE. The clock is connected using BUFGS so that there is negligible skew on the clock line. The internal connections of the counter are shown in the figure below. For this problem consider the parameters of the XC4000E-4 $T_{setup} = 4.0$ ns min, $T_{hold} = T_{CKI} = 0$ ns, $T_{CKO} < 3.7$ ns, and inverter plus interconnect propagation 6 ns. (That is, delay from Q_1 through interconnect and inverter to D_0 is 6 ns). Delays are $T_0 = 15$ ns, $T_1 = 75$ ns, and $T_2 = 10$ ns.

a. Determine the maximum clock speed using a timing diagram, showing clock, Q_0, D_1, Q_1, D_0.

b. Consider the clock signal running at 2 MHz. One of your colleagues has connected an unsynchronized input $COUNT$ to the CE (clock enable) inputs of the FDRE. Explain why this could be a bad idea by drawing a timing diagram, showing clock, $Q_0, D_1, Q_1, D_0, CE_0, CE_1, COUNT$. (I.e. show how setup time could be violated with COUNT being asserted at an inopportune time.)

c. An external system generates a high pulse on $COUNT$ lasting $500ns$. This pulse occurs at a random time (uniform distribution). Quantitatively estimate the chance of a setup time being violated.

d. What can be done to significantly reduce the chance of a randomly occuring $COUNT$ pulse (of width 500 ns) violating setup times? Modify the circuit and show with a new timing diagram how it can handle the randomly occuring $COUNT$ pulse.



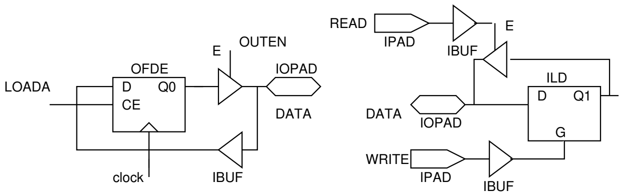
2. Xilinx Tristate IO (35 pts)

Consider the data path below consisting of a Xilinx output FF and a Xilinx input latch (level sensitive).

a. Draw a timing diagram, showing LoadA, Data, Read, Write, OutEn, and Clock, which will write data from OFDE into the input latch ILD, and then read data from ILD and store it into OFDE (without bus conflict ior other timing problems).

b. Using data from the IOB timing, (p. 4-103 to 4-107) estimate how fast the operation in part a could be performed.

c. If you were to design an FSM to control this operation, how many states would it need? Which signal(s) generated by the FSM need to be glitch free? How could these glitch free outputs be generated?



3. Lead Inductance/Ground Bounce (15 pts)

Suppose a Xilinx 4005E-4 chip has 32 outputs driving 20 pF loads each.

a. What is the peak power supply current required just for driving the load capacitance for slow and fast slew rate CMOS drivers?

b. Why should long thin wires be avoided for power supply connections to the Xilinx chip?