Professor Fearing EECS150/Problem Set 5 Fall 1998

Due at 10 am, Fri. Oct. 2 in box outside 218 Cory Hall

Quiz 1. 2-330 pm Tues. Sep. 29, 10 Evans

Reading Katz: 4.2

1. Glitches (20 pts)

Consider the x74_163 component from the Xilinx library, with the counter counting 0,1,2,...,14,15,0,1, ... (Also see text p. 353-356). A NOR gate is used to detect state 0 ($ZERO = \overline{Q_3 + Q_2 + Q_1 + Q_0}$). The delay from the output of each flip-flop in the counter to the NOR gate driving ZERO depends on the layout chosen by the xilinx place and routing software. Assuming variable timing delays, show with a timing diagram all places where glitches could be generated on transitions. What would happen if the ZERO signal were used to drive the asynchronous reset input of another counter?

2. Clock Skew (30 pts)

For this problem consider the parameters of the XC4000E-4 $T_{setup} = 4.0$ ns min, $T_{hold} = T_{CKI} = 0$ ns, $T_{CKO} < 3.7$ ns, $T_{delay} = 20$ ns and inverter plus interconnect propagation 6 ns. (That is, delay from Q_1 through interconnect and inverter to D_0 is 6 ns).

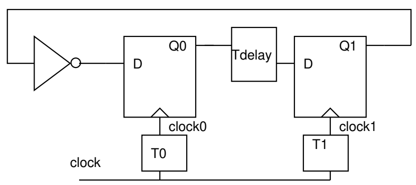
For each question below, justify your answer with a timing diagram.

a. With delay $T_0 = T_1 = 0$ ns, what is the maximum clock speed?

b. What is the maximum $T_1 - T_0$ for proper operation?

c. What is the minimum $T_1 - T_0$ for proper operation?

d. In Xilinx XC4000 designs, how can you prevent indeterminate delays on the clock line due to random routing?



3. Controller Design and Tri-state busses (50 pts)

Assume a delay of 5 ns from E being deasserted to the buffer being tri-stated, and a delay of 15 ns from E being asserted to the buffer being active. The data path is 8 bits wide.

a. Draw a timing diagram (showing signals LOADA, LOADSUM, ENADD, LOADACC, ENACC, Data Bus and Φ) which will replace the contents of the accumulator with 5 times the original value. Make sure that there are no bus conflicts, and that you allow reasonable setup and hold times for all devices.

b. Design a controller circuit, which given a START signal will perform the multiplication, then assert DONE until the next START signal is input. (Hint: use counter plus decoder plus appropriate logic). Show state and logic diagrams for controller.