Professor Fearing   EECS150/Problem Set 3   Fall 1998

Due at 5 pm, Fri. Sep. 18 in box outside 218 Cory Hall

Reading Katz: 7.1:7.3, 10.3.4, lab reader: XC4000E p.4-9 to 4-11, 4-21 to 4-22, 4-29 to 4-35

1. Counter Design (10 pts) (more practice)

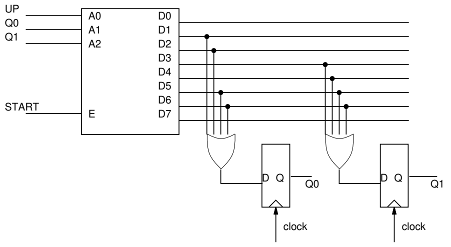
Using 3 type D flip-flops and extra logic, design a 3 bit counter which counts in the sequence $Q_2Q_1Q_0 = 0, 1, 3, 2, 6, 7, 5, 4, 0, \ldots$. Show state diagram, state transition table and schematic diagram.

2. Xilinx Combinational Logic Block (CLB) (25 pts)

Xilinx states that the XC4005 CLB F and G look up tables can perform any 4 input logic function, and the H box can perform any 3 input function. Prove that using the F,G, and H look up tables, you can calculate ANY function of 5 variables. (see Fig. 2, p. 4-10 in Xilinx manual).

3. FSM Analysis (25 pts)

Determine the state transition table and draw the state diagram for this FSM:



4. Parallel-to-Parallel Converter (40 pts)

Design a system which can convert 8 parallel input bits (DataIn[7:0]) to a serial output SerialOut. The system operates as follows. A clock signal is provided which is synchronized with DataIn[7:0]. When START is asserted, the system should first load the 8 bits, then shift out 8 bits (one bit per clock cycle), then stop shifting and assert the DONE signal. The data path of the system should use an 8 bit shift register and 3 bit counter from the Xilinx library, and any other necessary combinational logic. (The 3 bit counter keeps track of when 8 bits have been shifted out). (You will probably wish to use just 3 bits of a 4 bit counter as the library does not have 3 bit counters). The control section should use a D FF based Mealey FSM to keep track of whether the system is waiting for START or shifting.

In addition to schematic, show a timing diagram of operation, and state diagram for the controller FSM.