Professor Fearing EECS150/Problem Set 2 Fall 1998

Due at 5 pm, Fri. Sep. 11 in box outside 218 Cory Hall

Reading Katz: 6.1, 8.2, 8.4, 8.5

1. Combinational Logic Design (20 pts)

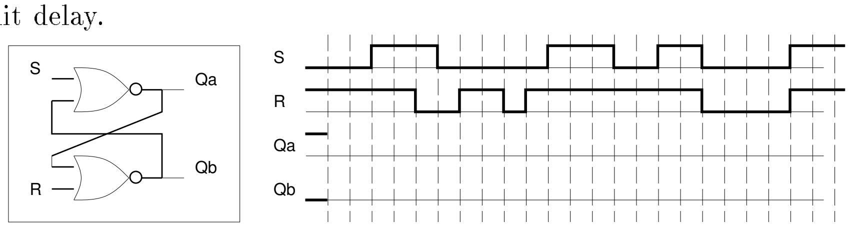
a. Design a combinational circuit that will compare two bits A and B and generate 3 outputs: i) min(A,B), ii) $A < B$, iii) $A = B$. This circuit must be designed such that it is modular and can be cascaded.

b. Show how to interconnect your 1 bit modules to implement a combinational logic system which will take as input two 8 bit numbers A[7:0] and B[7:0] and output 8 bits representing the minimum of A and B.

c. Assuming unit delay for all gates and inverters, calculate the worst case delay for calculating the 8 bit min.

2.Set-Reset Latch Timing (20 pts)

Complete the timing diagram for the latch below, assuming unit delay through the gates. The grid spacing is one unit delay.



3. Finite State Machine Analysis (20 pts)

Make a state transition table and state diagram for an FSM with a state register consisting of two D type FF, and input signal A. The next state equations (equivalently, inputs to the FF) are: $D_0 = \bar{A} + \bar{Q}_1 \oplus Q_0$ and $D_1 = \bar{Q}_1 + Q_0$.

4. Counter Design (20 pts)

Using 3 type D flip-flops and extra logic, design a 3 bit counter which counts in the sequence $Q_2Q_1Q_0 = 0, 1, 2, 4, 6, 3, 5, 7, 0, \ldots$. Show state diagram, state transition table and schematic diagram.

5. FSM Design (20 pts)

This problem examines a sequential logic approach to the minimum function described in problem 1. The finite state machine has as inputs two synchronized serial bit streams A and B, presented with most significant bit first. At each clock, the output of the FSM should be the bit stream (A or B) with the minimum value. The operation is shown in the timing diagram below.

Draw a state diagram, state table, and logic diagram for a Mealey type FSM which implements this function. You will probably need a global reset signal to initialize the FSM.