Professor Fearing EECS150/Problem Set 12 Fall 1998

Due at 10 am, Fri. Dec. 4 in box outside 218 Cory Hall

(This problem set may be done individually or by a group of two people maximum.)

1. State Partitioning (30 pts)

Katz 9.14.

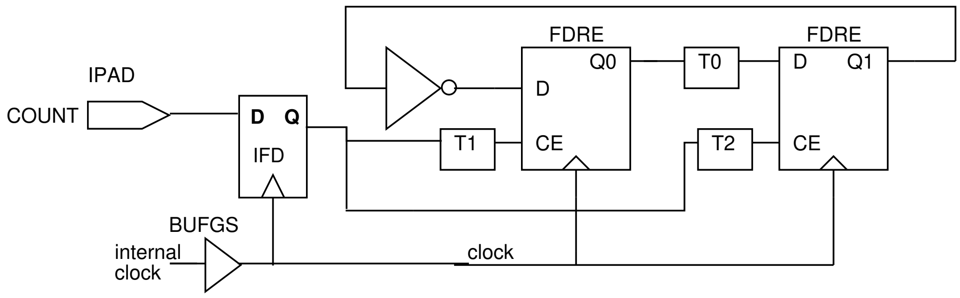
2. Metastability (50 pts)

This question considers the problem of a synchronizer FF going metastable and causing an FSM to have an incorrect next state. Consider a FSM as shown in the block diagram below, using the Xilinx 4005E-4. Assume COUNT (an unsynchronized input) is at 20 KHz and Clock is at 20.0 MHz. For this problem consider the parameters of the XC4005E-4 $T_{setup} = 4.0$ ns min, $T_{hold} = T_{CKI} = 0$ ns, $T_{CKO} = 3.5$ ns, and inverter plus interconnect propagation 12 ns. (That is, delay from Q_1 through interconnect and inverter to D_0 is 12 ns). Delays are $T_0 = 15$ ns, $T_1 = 20$ ns, and $T_2 = 30$ ns. The input FF has propagation delay $T_{IKRI} = 5.6ns$.

a. Draw a detailed timing diagram for the FSM. What is the maximum metastable time Δ_o for proper FSM operation?

b. What is the metastability failure probability rate for this clock and data rate, and the timing in part a? (Assume parameters for IFD $K_1 = 1.5 \times 10^{-10} sec$ and $K_2 = 3.7 \times 10^{9} sec^{-1}$.)

c. Now assume that there is an additional 8 ns delay, so that T_2 now equals 38 ns. Now what would the failure rate be?



3. Testability (20 pts)

Which nodes in the circuit below can not be completely tested for functionality by setting inputs ABC and observing output Y? Is the unobservable fault(s) stuck-at-one or stuck-at-zero?