Professor Fearing EECS150/Problem Set 11 Fall 1998

Due at 10 am, Fri. Nov. 20 in box outside 218 Cory Hall

(This problem set may be done individually or by a group of two people maximum.)

1. K-maps (40 pts)

With a four digit binary input number $A_3A_2A_1A_0$, design a circuit that generates a 4 bit output code $BC.DE_2$ which is the logarithm base 2 of the input. For example if the input is 6 (0110_2), $log_2(6) \approx 2.59 \approx 10.10_2$ thus the four output functions should be $B = 1$, $C = 0$, $D = 1$, and $E = 0$. The inputs and outputs are Asserted High. The input 0 is not allowed, so the outputs for $A_3A_2A_1A_0 = 0000$ are don't care.

- Define the truth table for the four functions.
- Show all Karnaugh maps for S.O.P. and P.O.S.
- Draw the logic diagram using NAND gates only for minimized S.O.P. (Follow the bubble matching conventions).
- Draw the logic diagram using NOR gates only for minimized P.O.S. (Follow the bubble matching conventions).

2. State Minimization (40 pts)

Given the state diagram of Figure Ex9.4 (Katz pg. 489), use the state implication method to find and draw the fully reduced state diagram. What strings cause the recognizer to output a 1?