Professor Fearing EECS150/Problem Set 1 Fall 1998

Due at 5 pm, Fri. Sep. 4 in box outside 218 Cory Hall

Reading Katz: App. A, 5.1, Ch. 1, 2:2.2, 2.5, 3.1.1

1. (10 pts) Perform the following number system conversions:

a. $11010101_2 = ?_8 = ?_{10} = ?_{16}$ b. $110.111_2 = ?_8 = ?_{10} = ?_{16}$

c. $?_2 = ?_8 = 150_{10} = ?_{16}$ d. $?_2 = ?_8 = ?_{10} = A8.F_{16}$

e. $?_2 = ?_8 = ?_{10} = 241_{16}$

2. (10 pts) Arithmetic:

Showing your calculations, add 180_{10} and 171_{10} in base 2, 10, and sixteen.

Showing your calculations, multiply 223_4 and 103_4 in base 2, 10, and sixteen.

3. (10 pts) Modulo arithmetic. Calculate the following:

a. 105_{10} (mod 8) = $?_{10}$ b. 105_{10} (mod 4) = $?_{10}$

c. Does x (mod 16) plus y (mod 16) equal $(x + y)$ (mod 8)?

4. (15 pts) Reduce the following Boolean expressions using theorems and identities:

a. $F = AB(C + \bar{C}) + A\bar{B}$

b. $F = AB + BC\bar{D} + \bar{A}C\bar{D}$

c. $F = \overline{A\overline{(B + C)}D}$

d. $F = \overline{A \cdot \bar{B} \cdot \bar{C}}$

e. $F = (A + B)(\bar{A} + B + C)(\bar{A} + B + \bar{C})$

5. (20 pts) Implement $F.L = AB + C\bar{D}$ with all inputs asserted low (i.e. inputs are $A.L, B.L, C.L, D.L$) using:

a. AND, OR, and INVERTER gates.

b. only NAND gates

c. only NOR gates

(See fig. 2.60 in Katz for alternative symbols for gates, which should help in thinking about implementation).

6. (20 pts) Subtractor.

a. Write the truth table for a one-bit full subtractor which has inputs A, B, BorrowIn, and outputs D and BorrowOut.

b. Write the logic equations for D and BorrowOut.

c. Implement logic for D and BorrowOut using AND, OR, and INVERTER gates.

7. (15 pts) Timing.

Assuming unit delay for the INVERTER and OR gate, sketch a timing diagram showing $A, A1, Y$. Assume A is zero for 4 time units, goes to 1 for 4 time units and then returns to zero for 4 time units.