Preliminary Syllabus for EECS 150, Fall 1997
Prof. Fearing
Text: R.H. Katz, *Contemporary Logic Design*

Date	Lecture Topics	Reading-Katz	Lab
26 Aug	Boolean Algebra, numbers, symbols	App. A, 5.1 Ch. 1, 2:2.2	
28 Aug	combinational logic	2.5	
2 Sep	state elements	6.1	Lab 1
4 Sep	finite state machines	8.1, 8.2, 8.4, 8.5	Intro. to Viewlogic
9 Sep	counters, shift registers	7.1:7.3	Lab 2
11 Sep	FPGA Overview	10.3.4, reader	FSM
16 Sep	design examples	8.5, 10.4	Lab 3
18 Sep	timing and logic analyzer	6.1, 6.2	FPGA
23 Sep	busses, mux, tri-state	4.2	Lab 4
25 Sep	quiz review		Instrumentation
30 Sep	QUIZ 1		Lab 5
2 Oct	wiring considerations	(Wakerly 8.4)	Shift Reg. and Counters
7 Oct	RAM and ROM	7.6, 4.2.5	Lab 6
9 Oct	serial communications		Nasty Realities
14 Oct	video interface, A/D		Lab 7
16 Oct	top-down design, synch design		SRAMS
21 Oct	computer data paths	11:11.2	Checkpoint 1
23 Oct	computer control units I	11.3	
28 Oct	micro-programming	12.3:12.4	Checkpoint 2
30 Oct	computer control units, II	12:12.6	
4 Nov	computer arithmetic, quiz review	5.2:5.7	Checkpoint 3
6 Nov	QUIZ 2		
11 Nov	logic minimization, K-maps	3.1:3.3	Checkpoint 4
13 Nov	FSM optimization	9:9.5	
18 Nov	metastability, arbiter, hazards	3.4, 6.4	Checkpoint 5
20 Nov	testability		
25 Nov	error correction, handshaking	6.5	
27 Nov	Happy Thanksgiving		
2 Dec	HDTV		Proj. Demo deadline
4 Dec.	final review		Proj. Report Due