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Lab 6
Nasty Realities

1 Objectives

For this lab, you will learn about

1. capactive loading and its effect on propagation delays
2. transmission lines and termination for long wires
3. capacitive coupling on ribbon cables

2 Prelab

All of the activity involved in this lab takes place in room 204B. Note that there is no way to work on this lab in advance, so read this writeup carefully so that you will know what to do when your lab section begins. If you are still confused, please ask a TA *before* the start of your lab section.

3 Overview

Much of engineering is knowing what you can ignore. For example, we ignore the behavior of electrons in a digital circuit and think instead of 1's and 0's. This approximation has proven very successful, but it is important to know when we can no longer make it, or what to do to ensure that we can make it. Here are some of the assumptions we have been making:

- Wires are ideal – at any point in time, the voltage at every point on the wire is the same.
- There are exactly two logic levels – high and low.
- Transitions occur instantaneously from one voltage level to the next.

This lab is broken into two large experiments. Section 5 discusses the concepts of propagation delay and capacitive loading. Section 5.4 describes the associated experiment. Section 6 discusses the nasty realities of wires; Section 6.5 describes the associated experiment. Section 4 describes some of the miscellaneous things you need to know in order to build the circuits in this lab.

4 Details

4.1 Breadboard

We will use a breadboard to build the circuits for this lab. A breadboard is simply a slab of plastic, covered with holes connected by hidden metal contacts. By pushing stripped ends of wire, leads of discrete components, or IC pins into these holes connects them electrically to anything in the same column.

The connections inside the breadboard are shown below in Figure 1a. Use the rows of connected holes for power and ground; use the columns for your circuit. Note that there is a break in the connection between the horizontal buses, located exactly halfway across the board. Put chips horizontally in the wide space separating the two columns of connections. Their pins should fit in the lowest row of the upper columns and the upper row of the lower columns.

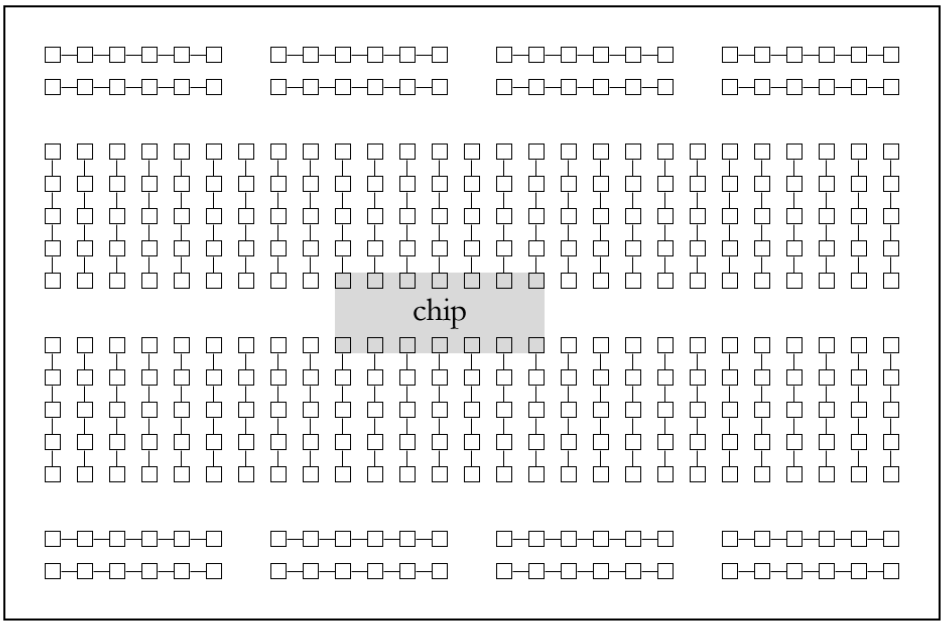

Figure 1a Breadboard connections

Power the circuits in this lab with the HP E3630A power supply that we used in Lab 4. Connect it to the banana jacks attached to the breadboard, and run wires from the jacks to the breadboard's power/ground buses. Clamp the wires to the jacks by unscrewing the top of the jack, threading a stripped wire end into the exposed hole, and screwing down the top of the jack.

4.2 Ribbon Cable

Some of the circuits in this lab use a long (ten foot) ribbon cable, which is a flat strip of insulated parallel wires. Adjacent wires in the cable alternate between connecting to the top and bottom pins of a 16-pin DIP connector, shown in Figure 1b.

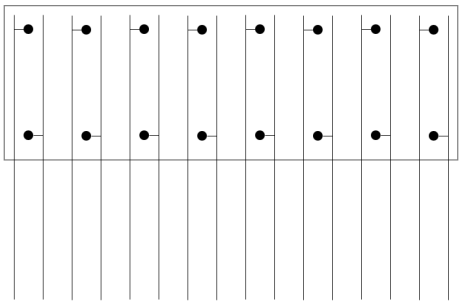

Figure 1b Ribbon cable DIP plug

4.3 Resistors and Capacitors

Discrete resistors, which you will be using in this lab, are marked with a code consisting of three colored bands. Each color corresponds to a number, as listed below.

Black	Brown	Red	Orange	Yellow	Green	Blue	Violet	Grey	White
0	1	2	3	4	5	6	7	8	9

The first two bands represent the first two digits of the resistance, and the third represents the number of zeroes following the first two numbers. For example, a resistor labeled yellow-violet-red would be interpreted as 4700 **Ω**, or 4.7 k**Ω**. The last band (gold) indicates a tolerance of 5%.

Capacitors are labeled similarly, although usually with three digits rather than colored bands. The number you obtain is the number of picofarads (pF). For example, a capacitor labeled "104" corresponds to 100000 pF, or 0.1 μF.

5 Transients and Delay Measurement

5.1 Propagation Delay

Contrary to what simulation software would have you believe, logic levels do not change instantaneously. A transition from 0 to 5 V or vice-versa requires a gradual change from one voltage to the next. In reality, what happens is that a capacitor is being charged or discharged to produce the output voltage. This unit of time is called the propagation delay.

The propagation delay t_p of a gate defines how quickly it responds to a change at its input. That is, the propagation delay expresses the delay experienced by a signal when passing through a gate. It is measured between the 50% transition points of the input and output waveforms. Because a gate usually displays different response times for rising or falling input waveforms, two definitions of the propagation delay are necessary. The t_{pLH} defines the response time of the gate for a low to high (or positive) output transition, while t_{pHL} refers to a high to low (or negative) transition. The overall propagation delay is conservatively defined as the maximum of the two delays t_{pLH} and t_{pHL}.

5.2 Capacitive Loading

The propagation delay of a gate is largely dependent on the capacitance that it must drive. This means that if one gate tries to drive many others, its capacitive load will be large. The incremental delay is directly related to the load capacitance; that is, each additional load inverter would add a constant amount to the overall delay. We use the term "fan-out" to refer to the number of load gates N that are connected to the output of the driving gate. The larger the fan-out, the longer the propagation delay.

5.3 Ring Oscillator

A standard circuit for delay measurement is the ring oscillator, which consists of an odd number of inverters connected in a circular chain. Due to the odd number of inversions, this circuit does not have a stable operating point, so it oscillates. The period T of the oscillation is determined by the propagation time of a single transition through the complete chain, or $T = 2 \times t_p \times N$, with N being the number of inverters in the chain. The factor 2 results from the observation that a full cycle requires both a low-to-high and a high-to-low transition.

5.4 To Do

We will build a ring oscillator and observe the output on the oscilloscope, enabling us to calculate the t_p for a single inverter. We will then add additional capacitive loads on the individual inverters and observe the effect on the ring oscillator frequency.

1. Build the ring oscillator circuit in Figure 2a on your breadboard. Use a 74F04PC hex inverter chip, whose pinout is shown in Figure 2b. Remember to connect pin 14 to +5V and pin 7 to ground!

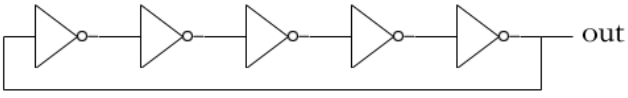

Figure 2a 5-stage ring oscillator

2. Using the oscilloscope, observe the output at pin 2 (actually, any of the five inverter outputs will do). Due to the extremely fast transitions, your output waveform will not look like a clean, sharp square wave as you might expect. Instead, you should see a very smoothed-out version of a square wave. Measure the period T of the ring oscillator and calculate the t_p for a single inverter. Record this value on the checkoff sheet and show your waveform to the TA.

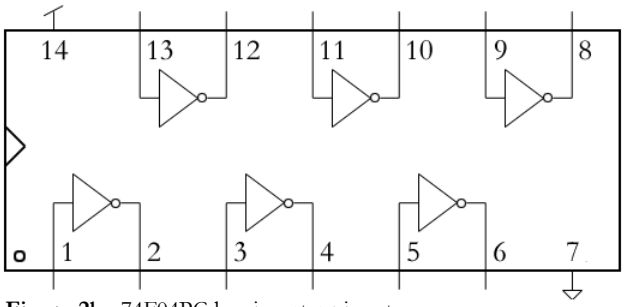

Figure 2b 74F04PC hex inverter pinouts

3. Connect a 100 pF capacitor from pin 4 to ground. What effect does this have on T? Now, connect additional load capacitors from pin 6 to ground, and pin 8 to ground. After adding each capacitor, measure the ring oscillator period. Record these three values on the checkoff sheet, and show that the relationship between load capacitance and propagation delay is roughly linear. Show your final waveform to the TA.

6 Wires

6.1 Nasty Realities

The nasty reality of wires is that they have "parasitic" resistance, capacitance, and inductance. Usually, these so-called parasitics are small enough to ignore, but when a wire is very long, or when a very high-speed signal is being applied, their effects can dominate.

Figure 3 is a model of these parasitics. The resistors are due to the wire conducting imperfectly, the capacitors are due to nearby conductors, and the inductors are due to current in the wire producing a magnetic field.

The parasitic capacitance slows a wire's response to a sudden change in voltage, and the parasitic inductance slows the response to a sudden change in current. Most digital logic lines conduct little current, but require the voltage to change frequently. Power supply lines have the opposite problem: their voltage is constant, but when many things change suddenly (i.e. when the clock rises), a sudden burst of current is required.

Together, inductance and capacitance make the wire behave as a *transmission line*, making signals travel at finite speed along the wire rather than being instantly sent. This is unimportant at low frequencies, but can become a problem at high frequencies. The speed of light, just under a foot per nanosecond, is a fundamental limitation – the clock period of today's 100 MHz digital circuits is just 10 ns.

The resistance is due to the wire being an imperfect conductor. At high currents, such as those on power wires, this can become a problem. At high frequencies, the resistance coupled with the inductance and capacitance forms a filter, causing the signal to "smear" as it travels along the wire.

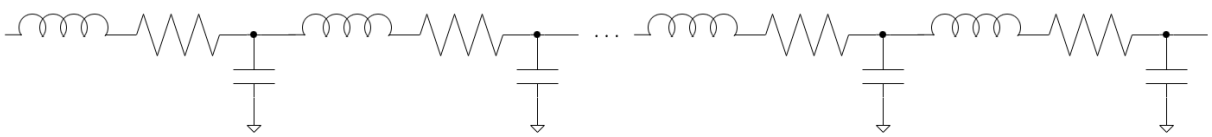

Figure 3 More realistic model of a wire

6.2 Termination

Reflections are a big problem in transmission lines. Like the rope analogy demonstrated in class, signals traveling along a transmission line can reflect at the end of a wire and interfere constructively, causing large voltage spikes. When a transmission line is short, reflection does not play a major role. However, when the line is sufficiently long, fast transitions on the input cause the traveling wave to "bounce back" from the opposite end.

Proper termination can eliminate reflections. Connecting a resistor with a value equal to the characteristic impedance of the transmission line is the simplest form of termination. This causes signals traveling along the transmission line to dissipate in the resistor; thus, reflection is eliminated. Ribbon cable (what you will use in today's lab) and twisted pair have a characteristic impedance of about 100 Ω. RG-58 coaxial cable, which we used to connect the signal generator to the oscilloscope in Lab 4, has a characteristic impedance of 50 Ω – incidentally, this is what the pulse generator expects to be driving.

6.3 Capacitive Coupling

There is capacitance between any two conductors, and wires running near each other are no exception. Figure 4 shows a model of capacitive coupling among three wires. Closer wires, in general, have more capacitance than wires further apart.

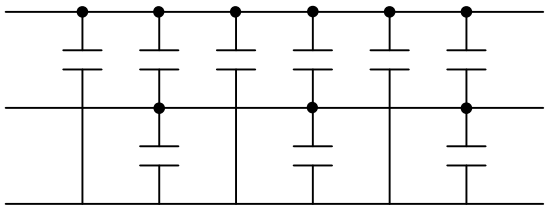

Figure 4 Capacitive coupling

Capacitors tend to keep the voltage between their terminals constant. This effect can induce a voltage/current spike on anything capacitively coupled when the voltage on a wire changes suddenly.

The capacitance between two conductors increases as they grow nearer and their common area increases. Thus, two long wires running parallel have more capacitive coupling than two short wires running orthogonally. This is unfortunate, since we often want to run many long wires near each other – most cables are like this.

6.4 Shielding

Shielding, or surrounding a wire with a grounded conductor, eliminates capacitive coupling. Coaxial cable is fully shielded: it consists of a central conductor for the signal surrounded by an insulator completely surrounded by a conductor – the shield. The problem with using coaxial cables for everything is that they are big and expensive.

Fortunately, incomplete shielding is often enough. Placing a grounded wire between two signal-carrying wires is a simple form of incomplete shielding that works well in practice.

6.5 To Do

1. Disconnect your ring oscillator circuit and hook up a 1 MHz 0-3V square wave from the 8112A pulse generator to the pin 1 of the hex inverter (actually, any inverter input will do). Hook up 50 Ω from this pin to ground – this presents the proper load to the pulse generator so that the voltage you set is the voltage you get. Use four 200 Ω resistors in parallel rather than a single 50 Ω resistor. Connect the output of the inverter to one of the wires on the ribbon cable.

2. Using the oscilloscope, measure the signal at the inverter input on channel 1, and measure the signal at the opposite end of the ribbon cable on channel 2. Use the metal base of the breadboard as a common ground for both your oscilloscope probes and the pulse generator. Compare the two signals – ideally, the

signal at the end of the ribbon cable would be a perfect inversion of the square wave. Is this the case? Why or why not?

3. Measure ΔV (including any overshoot) on both the high-to-low and low-to-high transitions on channel 2. Given that the output range of the 74F04 is approximately 0-3V, comment on the ΔV measured at the end of the transmission line. Are you getting positive or negative reflections? Estimate the reflection coefficient, and record it (along with ΔV) on the checkoff sheet and show the waveform to the TA.

4. Terminate the transmission line by placing two resistors at the end of the ribbon cable – 330 Ω to V_{CC} and 200 Ω to ground. Since these resistors are being placed in parallel with respect to the transmission line, the overall resistance is about 125 Ω. This value is sufficiently close to the characteristic impedance of the ribbon cable (100 Ω) for our purposes. How does this termination affect the waveform? Measure the new peak-to-peak voltage (Vpp), record it on the checkoff sheet, and show the waveform to the TA.

5. Leaving the rest of the circuit intact, select an unused inverter and connect its input to ground. Then connect its output, which should be V_{CC} (a DC signal), to the input of a wire two steps over – you will now have a square wave on one wire and V_{CC} on another, with one wire between them carrying no signal. Refer to Figure 1b to figure out which pin numbers correspond to which wires. On the oscilloscope, simulataneously display the V_{CC} signal at each end of the cable (use either a 2V or 5V scale on both channels). Your source waveform should be a fairly clean 5V signal, but the signal at the other end should display some oscillation. Explain why this happens.

6. Finally, connect the wire carrying no signal to ground, introducing a shield between the two signals. How does this affect the settling time and overshoot of the V_{CC} signal's oscillation? Show the TA the difference in the two waveforms and explain what is happening.

Name: _____ Name: _____

Lab Section (check one)
M: ❒AM ❒PM T: ❒AM ❒PM W: ❒AM ❒PM Th: ❒PM

7 Checkoff

1. Ring oscillator built (unloaded), waveform displayed on oscilloscope **TA:** _____(25%)

   t_p = _____

2. Capacitive loads added to ring oscillator, final waveform displayed on oscilloscope

   100 pF: $T_{overall}$ = _____

   200 pF: $T_{overall}$ = _____

   300 pF: $T_{overall}$ = _____ **TA:** _____(20%)

3. Square wave measured at end of ribbon cable

   ΔV = _____

   Estimated reflection coefficient = _____

   Explanation? **TA:** _____(20%)

4. Square wave measured at end of terminated ribbon cable, waveform displayed on oscilloscope

   Vpp = _____ **TA:** _____(20%)

5. Waveforms of V_{CC} with and without shielding displayed on oscilloscope

   Explanation? **TA:** _____(15%)

6. Turned in on time **TA:** _____(full credit)

7. Turned in one week late **TA:** _____(half credit)