Professor Fearing EECS150/Problem Set 9 Fall 1997

Due at 5 pm, Thu. Oct. 30 in box outside 218 Cory Hall

Quiz 2: Thurs. Nov. 6 in class.

1. (30 pts)

Katz Chapter 11, problem 4.

2. (40 pts)

Katz Ch 11, problem 13. (The register transfer micro-operations should show which bus is being used in the operation). You may want to improve the data path by adding $CBus \rightarrow PC$ and $MBR \rightarrow BBus$ connections.

3. (30 pts)

For the data path in Figure Ex11.13 in the text, list all the control signals required for full control of the processor. (Assume 4 control lines are sufficient for the ALU). Show with a timing diagram the operation of the processor during the **ADD Ra, (Rb)offset** instruction (see problem 2). Show CLOCK and all relevant control signals, and show data bus valid or tri-state times, labelling bus with contents, e.g. "bus=pc".