Professor Fearing EECS150/Problem Set 8 Fall 1997

Due at 5 pm, Thu. Oct. 23 in box outside 218 Cory Hall

1. Xilinx Stuff (20 pts)

a. What is a UPAD good for? How many are there in an XC4005 in 84 pin package like we are using? List some good uses for these extra flip flops.

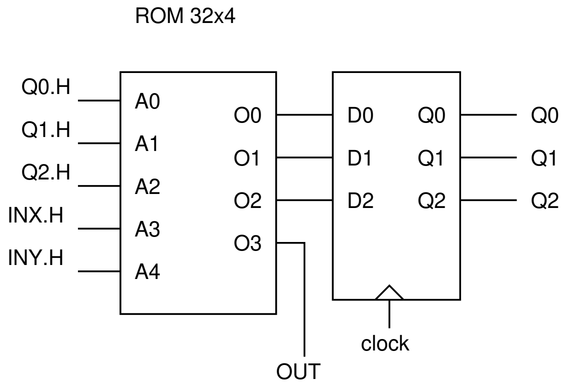
b. In what situation might you want to use an IPAD and IFD rather than an IPAD, IBUF, and FD?

2. Counter Design (25 pts)

Design a circuit, using appropriate up/down counters from the XC4000 Xilinx library which counts from 8 to 24 and then counts down to 8. (That is the sequence is 8,9,10,11, ..., 21,22, 23, 24, 23, 22, 21, 20, ..., 10,9,8,9,10, ...). Consider the counter blocks as your data path, and design a simple controller finite state machine which will control the up/down direction appropriately. Show a state diagram and timing diagram for your controller. Make your design fully synchronous, except possibly for an over-riding global asynchronous reset.

3. ROM Based FSM (20 pts)

Using the ROM based FSM shown below, with ROM contents as listed in Table 1, draw a state table and state diagram for the FSM. Explain why this is a Moore or Mealey type FSM. Consider synchronized inputs INX.H and INY.H. INY is asserted before the rising edge of clock cycle 0, then deasserted after the rising edge. Then the following data is presented in order at INX: 0,0,1,1,0,0,1,0,0. Draw a timing diagram showing CLOCK.H, INX.H, and OUT.H.



Adr	Data	Adr	Data	Adr	Data	Adr	Data
0	A	8	9	10	8	18	8
1	03	9	02	11	00	19	00
2	C	A	B	12	8	1A	8
3	05	B	04	13	00	1B	00
4	E	C	D	14	8	1C	8
5	07	D	06	15	00	1D	00
6	8	E	F	16	8	1E	8
7	01	F	00	17	00	1F	00