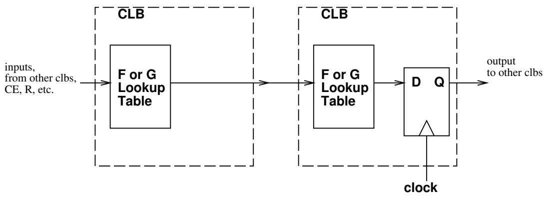
Professor Fearing EECS150/Problem Set 6 Fall 1997

Due at 5 pm, Thu. Oct. 9 in box outside 218 Cory Hall

1. Synchronization (60 pts)

This question illustrates the potential problems caused by feeding asynchronous inputs into a FSM. (Even ignoring metastability). Consider a digital system implemented using a Xilinx 4005-4 containing a 4 bit binary counter CB4RE. The clock is connected using BUFGS so that there is negligible skew on the clock line. A piece of the internal connections of the counter is shown in the figure below. Assume that the next state decoder for the uses a maximum of two look up tables as shown.

a. Using timing information from p. 2-53 in the Xilinx manual, estimate the maximum clock speed using a timing diagram. Assume a uniform 5 ns delay for the interconnection between CLBs.
b. Consider the clock signal running at 5 MHz. One of your colleagues has connected an unsynchronized input to the CE (count enable) line. Assume a uniform 5 ns delay for the interconnection between CLBs.
Explain, with the aid of a timing diagram, why this could be a bad idea. (I.e. show how setup time could be violated). Quantitatively estimate the chance of a setup time being violated. What might the counter do if setup time is violated?
c. Again consider the clock signal running at 5 MHz, and an unsynchronized input to the CE (count enable). Now assume that the interconnection delays between CLBs are no longer identical, and could be between 2 ns and 10 ns. Explain, with the aid of a timing diagram, how setup times could be violated. Quantitatively estimate the chance of a setup time being violated.



2. Propagation Speed and Reflections (25 pts)

A computer data/address bus is 0.5 meter from end to end. The CPU board is at one end of the bus and a memory board is at the other end. (Assume $c_{bus} = 2 \times 10^8 ms^{-1}$).
a. If the bus is not properly terminated, what rise and fall times would be permissible on edges (rule of thumb)? What would the minimum time for a read-modify-write memory cycle be (assuming extremely fast CPU and memory board)?
b. With proper bus termination, what would the minimum time for a read-modify-write memory cycle be?

3. Lead Inductance (15 pts)

A high speed CMOS chip has been encased in a package with 1 nH lead inductance. If a single output sources or sinks 20 mA, and it is desired to limit inductive spikes to less than 0.5 V, how fast can the output switch from 5V to 0V or 0v to 5v? (Assume linear slope for the output current).