Professor Fearing EECS150/Problem Set 5 Fall 1997

Due at 5 pm, Thu. Oct. 2 in box outside 218 Cory Hall

Quiz 1. 2-330 pm Tues. Sep. 30, 10 Evans

Reading Katz: 4.2

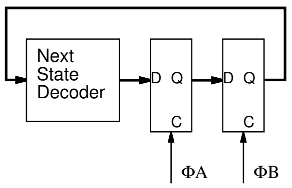
1. Glitches (20 pts)

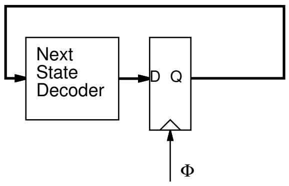
Consider the RCO ("ripple carry output") output of the x74_163 component from the Xilinx library, with the counter counting 0,1,2,...,14,15,0,1, ... (Also see p. 353-356). The delay from the output of each flip-flop in the counter to the AND gate driving RCO depends on the layout chosen in the xilinx chip. Assuming variable timing delays, show with a timing diagram how glitches could be generated on some transitions. What would happen if the RCO signal were used to drive the clock input of another counter?

2. Two Phase Clocking (30 pts)

a. Consider the state machine in the figure below, which uses two transparent latches, and two non-overlapping clock phases Φ_A and Φ_B. Assume the latches have hold time of 5 ns, propagation delay of 20 ns max, and the next state decoder has delay of 20 ns max. Determine, by drawing a timing diagram, the fastest frequency clock this circuit can use and still run reliably. Why do you need two latches instead of one?

b. Consider the state machine in the figure below, which uses an edge triggered state register. Assume the type-D FF have hold time of 5 ns, setup time 5 ns, and the next state decoder has delay of 20 ns max. Determine, by drawing a timing diagram, the fastest frequency clock this circuit can use and still run reliably.





3. Controller Design and tri-state busses (50 pts)

Assume a delay of 3 ns from T being asserted to the buffer being tri-stated, and a delay of 12 ns from T being deasserted to the buffer being active. The data path is 8 bits wide.

a. Draw a timing diagram (showing signals LOADA, LOADB, DISADD, LOADACC, DISACC and Φ) which will replace the contents of the accumulator with 3 times the original value. Make sure that there are no bus conflicts, and that you allow reasonable setup and hold times for all devices.

b. Design a controller circuit, which given a START signal will perform the multiplication, then assert DONE until the next START signal is input. Show state and logic diagrams for controller.