Professor Fearing EECS150/Problem Set 4 Fall 1997

Due at 5 pm, Thu. Sep. 25 in box outside 218 Cory Hall

Quiz 1. 2-330 pm Tues. Sep. 30, 10 Evans

Reading Katz: 6.1:6.2,8.5, 10.4

1. Combinational Logic (25 pts)

Your company is going to market a "dissipationless" processor using a bunch of "Fredkin gates", which are a 3-input 3-output function, with the truth table for the Fredkin gate shown to the right. They have great power dissipation, but a fanout of only one. (That is, the gate output can drive only one other gate). (They are interesting since they conserve the numbers of ones and zeros, and are reversible). For each of the following problems, you have available sources of zeros and ones and as many cascaded Fredkin gates as necessary.

Inputs			Outputs		
u	v	w	x	y	z
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	0	1
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	0	1
1	1	0	1	1	0
1	1	1	1	1	1

a). Implement the FAN-OUT function (i.e. if the signal A is applied to one of the inputs, determine connections such that two of the outputs will have the signal A applied).

b). Design a 2:4 decoder, that is, a circuit with 2 inputs and 4 outputs, say Y0, Y1, Y2, Y3. Y0 is asserted if the input is 0, Y1 is asserted if the input is 1, etc.

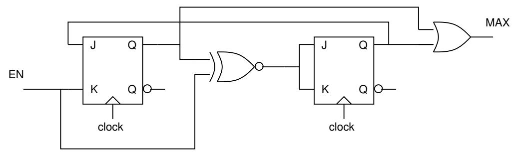
c) Design a 4:1 multiplexer, that is a circuit which uses two select lines to select one of 4 inputs.

2. FSM Design (25 pts)

Design a Moore type FSM for a sequence recognizer. The FSM should assert OUTPUT for one clock cycle for every (possibly overlapping) sequence "101" detected in the synchronized input data stream Z. Show timing diagram, state diagram, state table, and schematic using synchronous reset D-type FFs from the Xilinx library.

3. FSM Analysis (25 pts)

Make a state transition table and state diagram for the following circuit:



4. Timing Analysis (25 pts)

Using a timing diagram, determine the minimum clock period for this circuit. Also, determine the fastest inverter which could be used in this circuit. (Parameters: $T_{setup} = 5$ ns min, $T_{hold} = 10$ ns, $5 < T_{CKO} < 15$ ns, and inverter propagation $8 < t_p < 12$ ns.)