Professor Fearing EECS150/Problem Set 3 Fall 1997

Due at 5 pm, Fri. Sep. 19 in box outside 218 Cory Hall

Reading Katz: 7.1:7.3, 10.3.4, lab reader

1. Counter Design (25 pts)

Using 3 type D flip-flops and extra logic, design a 3 bit counter which counts in the sequence $Q_2Q_1Q_0 = 0, 3, 6, 1, 4, 7, 2, 5, 0, \ldots$. Show state diagram, state transition table and schematic diagram.

2. Xilinx Combinational Logic Block (CLB) (25 pts)

Xilinx states that the XC4005 CLB F and G look up tables can perform any 4 input logic function, and the H box can perform any 3 input function. Prove that using the F,G, and H look up tables, you can calculate ANY function of 5 variables. (see Fig. 1, p. 2-10 in Xilinx manual).

3. Serial-to-Parallel Converter (50 pts)

Design a system which can convert 8 serial input bits (SerialDataIn) to an 8 bit parallel output DataOut[7:0]. The system operates as follows. A clock signal is provided which is synchronized with SerialDataIn. When START is asserted, the system should shift in 8 bits, then stop shifting and assert the DONE signal. The parallel output of the shift register is DataOut[7:0]. The data path of the system should use an 8 bit shift register and 3 bit counter from the Xilinx library, and any other necessary combinational logic. (The 3 bit counter keeps track of when 8 bits have been shifted in). The control section should use a D FF based FSM to keep track of whether the system is running or Done.

In addition to schematic, show a timing diagram of operation, and state diagram for the controller FSM.

Serial Receiver Block Diagram