Professor Fearing EECS150/Problem Set 2 Fall 1997

Due at 5 pm, Fri. Sep. 12 in box outside 218 Cory Hall

Reading Katz: 6.1, 8.2, 8.4, 8.5

1. Combinational Logic Design (25 pts)

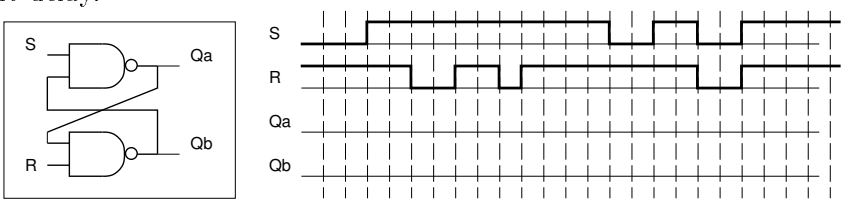
a. Design a combinational circuit that will compare two bits A and B and generate 3 outputs: i) max(A,B), ii) $A > B$, iii) $A = B$. This circuit must be designed such that it is modular and can be cascaded. You may need additional inputs to be able to cascade the modules.

b. Show how to interconnect your 1 bit modules to implement a combinational logic system which will take as input two 8 bit numbers A[7:0] and B[7:0] and output 8 bits representing the maximum of A and B.

c. Assuming unit delay for all gates and inverters, calculate the worst case delay for calculating the 8 bit max.

2. Set-Reset Latch Timing (25 pts)

Complete the timing diagram for the latch below, assuming unit delay through the gates. The grid spacing is one unit delay.



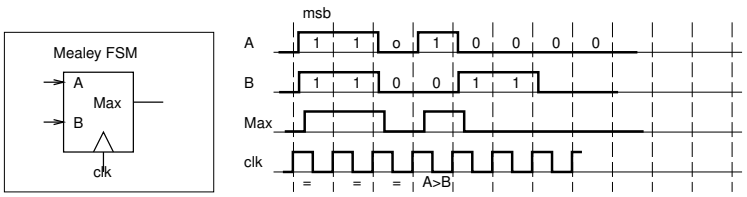
3. Finite State Machine (FSM) Analysis (25 pts)

You are given a mystery FSM with a state register consisting of two D type Flip-Flops (FF), and input signal A. The next state equations (equivalently, inputs to the FF) are:

$D_0 = \bar{Q}_0 \cdot A$ and $D_1 = Q_1 \oplus (Q_0 \cdot A)$.

Make a state transition table and state diagram for this FSM.

4. FSM Design (25 pts)

This problem examines a sequential logic approach to the maximum function described in problem 1. The finite state machine has as inputs two synchronized serial bit streams A and B, presented with most significant bit first. At each clock, the output of the FSM should be the bit stream (A or B) with the maximum value. The operation is shown in the timing diagram below.

Draw a state diagram, state table, and logic diagram for a Mealey type FSM which implements this function.