Professor Fearing EECS150/Problem Set 12 Fall 1997

Due at 5 pm, Thu. Dec. 4 in box outside 218 Cory Hall

1. State Partitioning (30 pts)

Katz 9.13.

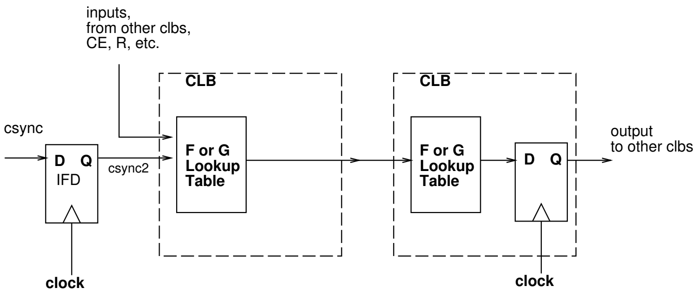
2. Metastability (50 pts)

This question considers the problem of a synchronizer FF going metastable and causing an FSM to have an incorrect next state. Consider a FSM next state decoder as shown in the block diagram below, using the Xilinx 4005-4. Assume Csync (an unsynchronized input) is at 15.75 KHz and Clock is at 16.0 MHz.

a. Using timing information from page 2-53 of the Xilinx manual, draw a detailed timing diagram for the FSM. The input FF has propagation delay $T_{IKRI} = 6.0ns$, and assume 10 ns interconnect delay from IOB to CLB and 10 ns from CLB to CLB. What is the maximum metastable time Δ_o for proper FSM operation?

b. What is the metastability failure probability rate for this clock and data rate, and the timing in part a? (Assume parameters are the same as in the handout for the XC3020-70, and that the IFD has the same properties as the CLB type D FF).

c. Now assume that there is an additional 25 ns delay in the path from the output of the IFD to the FSM compared to part a. (For example, 3 more combinational CLBs plus 13 ns total propagation delay.) Now what would the failure rate be?



3. Testability (20 pts)

Which nodes in the circuit below can not be completely tested for functionality by setting inputs ABC and observing output Y? Is the unobservable fault(s) stuck-at-one or stuck-at-zero?