Professor Fearing EECS150/Problem Set 11 Fall 1997

Due at 5 pm, Thu. Nov. 20 in box outside 218 Cory Hall

1. RAM Timing (review) (30 pts)

Consider the RAM data path from Quiz 2 Problem 4. Assume worst case 20 ns timing skew on all control lines, but negligible clock skew. Draw a detailed timing diagram for cases 1, 2, 3 and 6 showing all the given control signals and the databus contents, and show where all timing problems occur.

2. K-maps (20 pts)

With a three digit binary input number $A_2A_1A_0$, design a circuit that generates an output code $F_2F_1F_0$ which is the input minus 3 (output in mod 8). For example if the input is 2 (010_2) the three output functions should be $F_2 = 1$, $F_1 = 1$, and $F_0 = 1$. The inputs and outputs are Asserted High (A2.H, A1.H, A0.H)

- Define the truth table for the three functions.
- Show all Karnaugh maps for S.O.P. and P.O.S.
- Draw the logic diagram using NAND gates only for minimized S.O.P. (Follow the bubble matching conventions).
- Draw the logic diagram using NOR gates only for minimized P.O.S. (Follow the bubble matching conventions).

3. State Minimization (25 pts)

Given the state diagram of Figure Ex9.3 (Katz pg. 495), use the state implication method to find and draw the fully reduced state diagram. What strings cause the recognizer to output a 1?