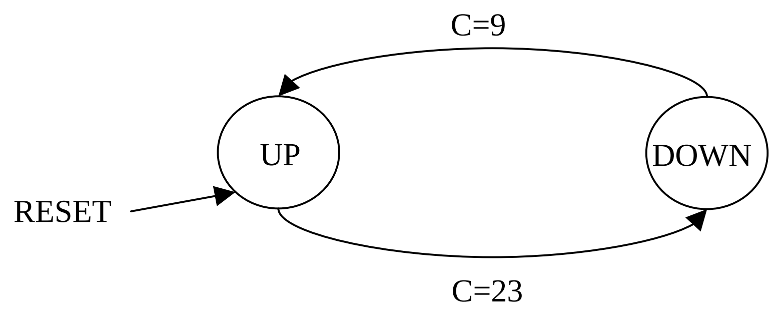
1.

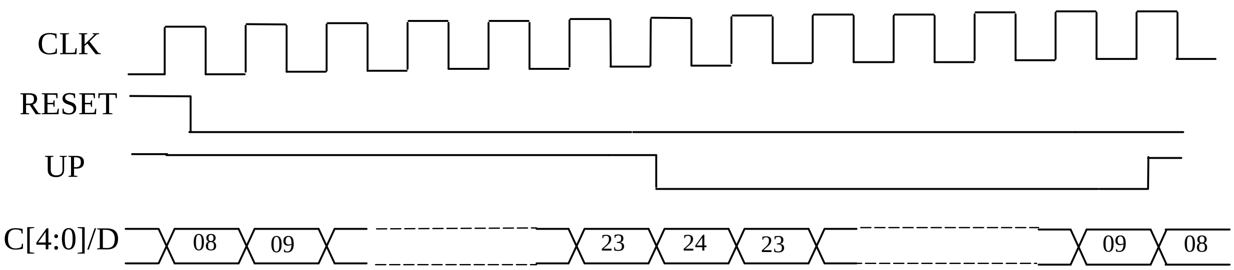
a. A UPAD allows the use of the any unbonded IOBs in a FPGA. There are totally 51 UPAD in an XC4005 in 84pin package. These extra flip flops can have inverted clock inputs and 3-state outputs. Also the outputs can be inverted or not inverted. They can be used in shift registers and temporary registers.

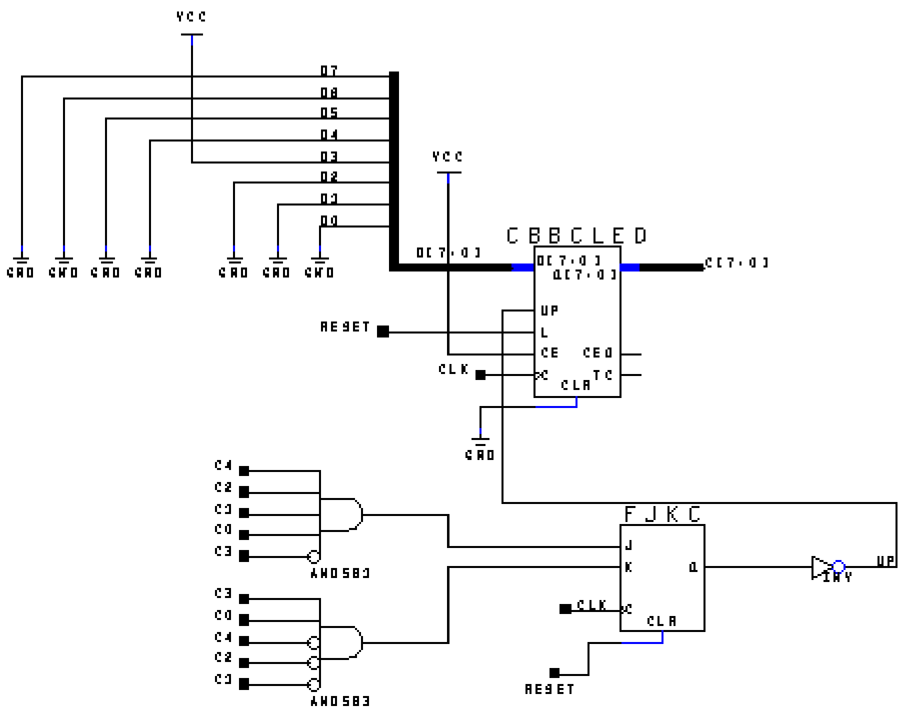
b. Since IPAD + IFD uses 1 IOB and 0 CLB, while IPAD+IBUF+FD uses 1 IOB and 1CLB, IPAD and IFD should be used instead of IPAD, IBUF and FD.

IFD can be used to synchronize the external input signal. Since the set-up time of the IFD can be configured, IPAD and IFD(set-up time is only 1.2ns) can be used for critical path, while the set-up time may be violated in the case of IPAD, IBUF and FD(2.8ns+7.3ns+wire-delay).

2.







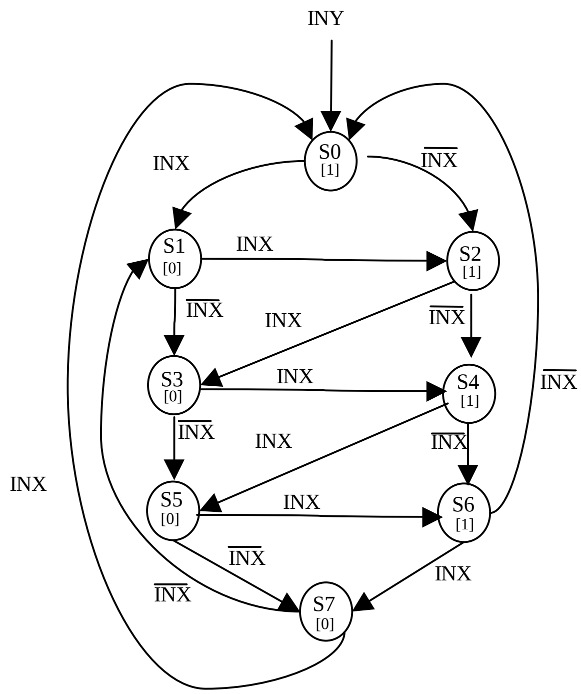
3.

INY.H	INX.H	Q2.H	Q1.H	Q0.H	OUT	Q2	Q1	Q0
0	0	0	0	0	1	0	1	0
0	0	0	0	1	0	0	1	1
0	0	0	1	0	1	1	0	0
0	0	0	1	1	0	1	0	1
0	0	1	0	0	1	1	1	0
0	0	1	0	1	0	1	1	1
0	0	1	1	0	1	0	0	0
0	0	1	1	1	0	0	0	1
0	1	0	0	0	1	0	0	1
0	1	0	0	1	0	0	1	0
0	1	0	1	0	1	0	1	1
0	1	0	1	1	0	1	0	0
0	1	1	0	0	1	1	0	1
0	1	1	0	1	0	1	1	0
0	1	1	1	0	1	1	1	1
0	1	1	1	1	0	0	0	0
1	0	0	0	0	1	0	0	0
1	0	0	0	1	0	0	0	0
1	0	0	1	0	1	0	0	0
1	0	0	1	1	0	0	0	0
1	0	1	0	0	1	0	0	0
1	0	1	0	1	0	0	0	0
1	0	1	1	0	1	0	0	0
1	0	1	1	1	0	0	0	0
1	1	0	0	0	1	0	0	0
1	1	0	0	1	0	0	0	0
1	1	0	1	0	1	0	0	0
1	1	0	1	1	0	0	0	0
1	1	1	0	0	1	0	0	0
1	1	1	0	1	0	0	0	0
1	1	1	1	0	1	0	0	0
1	1	1	1	1	0	0	0	0

If we define the states as

STATE	Q2	Q1	Q0
S0	0	0	0
S1	0	0	1
S2	0	1	0
S3	0	0	1
S4	1	0	0
S5	1	0	1
S6	1	1	0
S7	1	1	1

the state diagram will be



It is a Moore Machine since the OUT only dependents on the states.