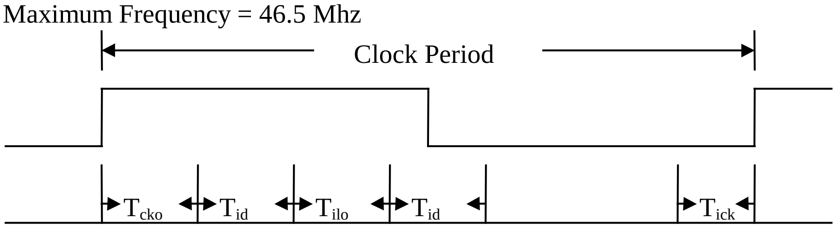
**R. Fearing and J. Shih EECS150 Problem Set 6 Solution Fall 1997**

1. Synchronization

a. Let

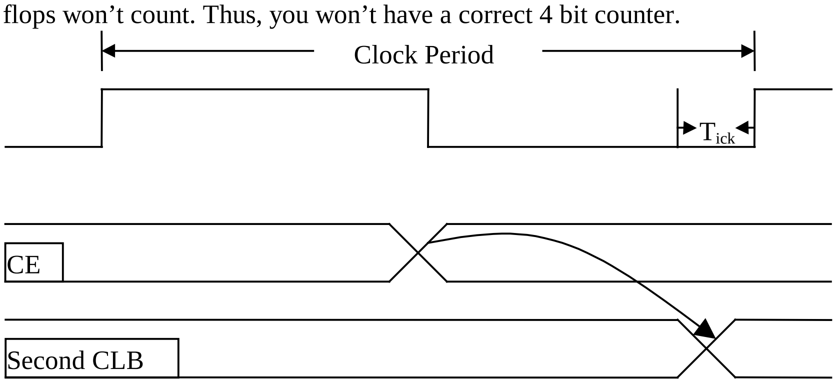
$T_{cko}$ = Sequential Delays from Clock K to outputs Q = 3.0 ns
$T_{id}$ = Interconnection Delays between CLBs = 5.0 ns
$T_{ilo}$ = Combinatorial Delays from F/G inputs to X/Y = 4.0 ns
$T_{ick}$ = Set-up Time before Clock K from F/G inputs = 4.5 ns

Minimum Clock Period > Propagation Delay + Setup Time = $T_{cko} + T_{id} + T_{ilo} + T_{id} + T_{ick}$ = 3.0 ns + 5.0 ns + 4.0 ns + 5.0 ns + 4.5 ns = 21.5 ns
Maximum Frequency = 46.5 Mhz




b.

The counter can go crazy if the setup time is violated. For example: if a change in CE causes the second CLB to miss its setup time requirement, then some counter flip flops will count while other counter flip flops won't count. Thus, you won't have a correct 4 bit counter.




Assume the minimum $T_{ilo}$ is 0.0 ns. Then the minimum propagation delay between CE and the second CLB is 5.0 ns ($T_{ilo} + T_{id}$ ) and the maximum propagation delay between CE and the second CLB is 9.0 ns ($T_{ilo} + T_{id}$). Thus the propagation delay can vary for 4.0 ns (9.0ns – 5.0 ns).
Therefore CE must be stable for 8.5 ns (4.5 ns for the $T_{ick}$ and 4.0 ns for the variance in propagation delay).
5 MHz => 200 ns clock period
8.5 ns / 200 ns = .0425 = 4.25%

c.

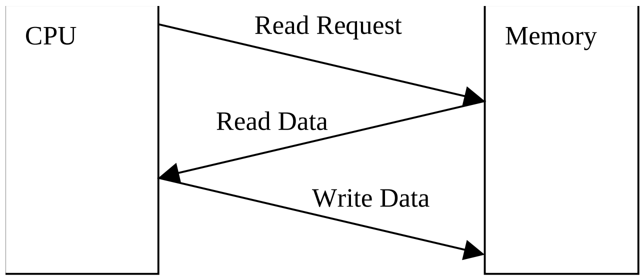
Assume the minimum $T_{ilo}$ is 0.0 ns. Then the minimum propagation delay between CE and the second CLB is 2.0 ns ($T_{ilo} + T_{id}$ ) and the maximum propagation delay between CE and the second CLB is 14.0 ns ($T_{ilo} + T_{id}$). Thus the propagation delay can vary for 12.0 ns (14.0ns – 2.0 ns).
Therefore CE must be stable for 16.5 ns (4.5 ns for the $T_{ick}$ and 12.0 ns for the variance in propagation delay).
5 MHz => 200 ns clock period
16.5 ns / 200 ns = .0825 = 8.25%

2. Propagation Speed and Reflections

Let

T = time for the signal to travel from one end of the bus to the other end
T = bus length / $c_{bus}$ = 0.5 m / $2 \times 10^8$ $ms^{-1}$ = 2.5 ns

A read-modify-write memory cycle requires sending data on the bus 3 times. (The first time to send the Read Request, the second time to get the Read Data back, and the third time to finish sending Write Data to Memory).




a. Without proper bus termination: each rise and fall time must be greater than 4T
=> a read-modify-write memory cycle requires 12T or 30 ns. (Neglecting transit time)
b. With proper bus termination: each rise and fall time must be greater than T
=> a read-modify-write memory cycle requires 3T or 7.5 ns. (Neglecting transit time)

3. Lead Inductance
$V=L\,(di/dt)$
$dt = (L/V)\,di$
$L = 1$ nH, $V = 0.5$ V, $di = 20$ mA
⇨ $dt = 4\times10^{-11}$ second

Things could be more serious if 100 outputs change simultaneously, then $dt > 4$ ns.