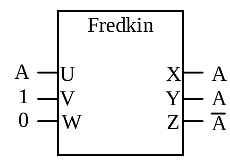
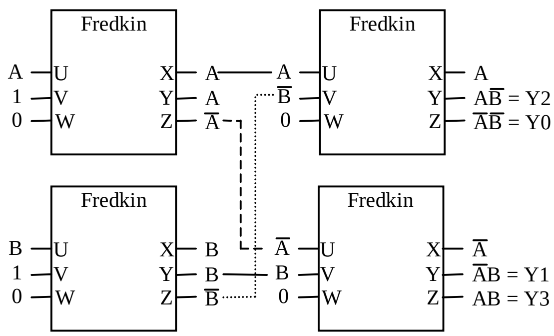
Problem Set 4 Solutions
Professor Fearing Fall 1997
Solutions created by Norman Walker

1.
From the truth table
$X = U$
$Y = W\overline{U} + VU$
$Z = V\overline{U} + WU$

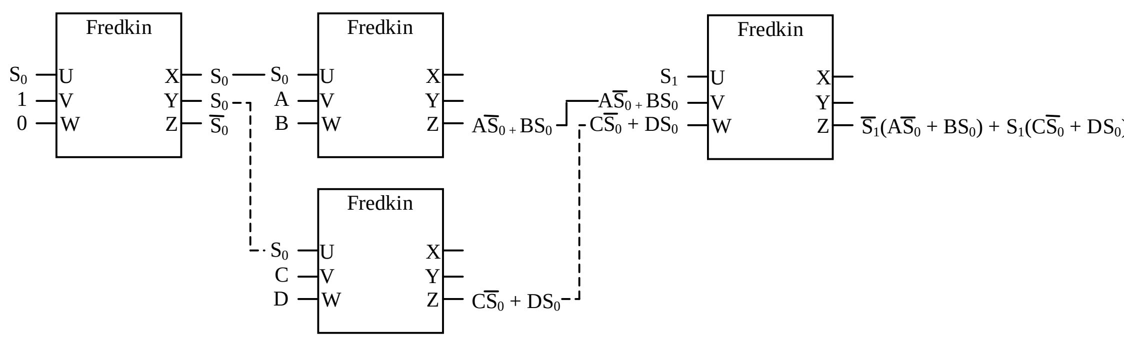
a.
If U = A, V = 1, & W = 0 then
$X = A$
$Y = A$
$Z = \overline{A}$



b.
For decoder you need: AB, $\overline{A}B$, $A\overline{B}$, & $\overline{A}\overline{B}$

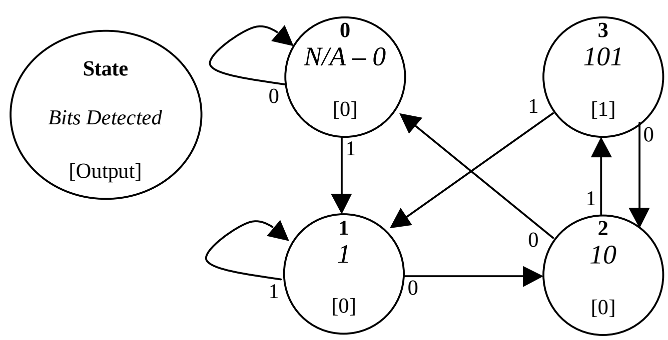


c.
For a 4:1 Mux you need: $\overline{S}_1(A\overline{S}_0 + BS_0) + S_1(C\overline{S}_0 + DS_0)$



2.

Q_1	Q_0	Z	Q_1^*	Q_0^*	OUT
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	1	0	0
0	1	1	0	1	0
1	0	0	0	0	0
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	0	1	1

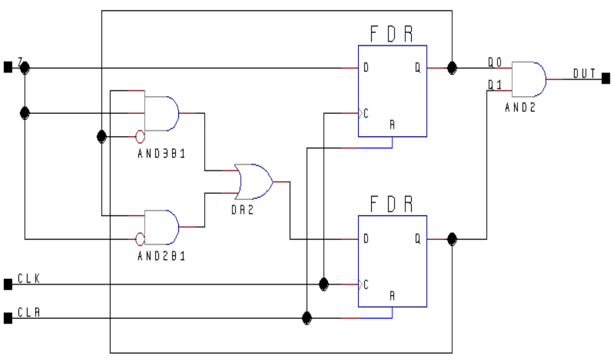


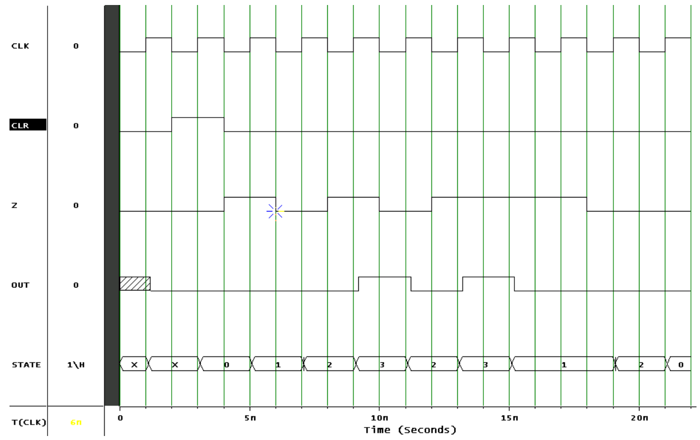
Equations

$Q_1^* = \overline{Z}Q_0 + ZQ_1\overline{Q}_0$

$Q_0^* = Z$

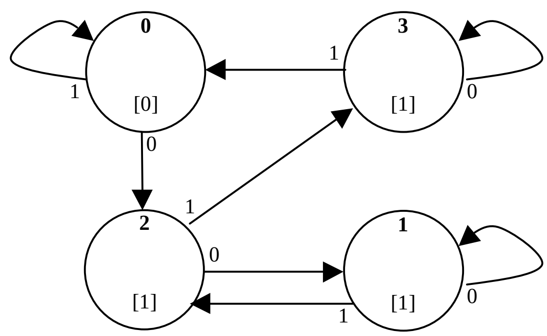
$OUT = Q_1Q_0$



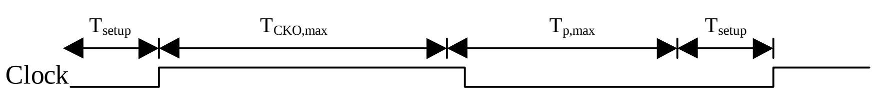


3.

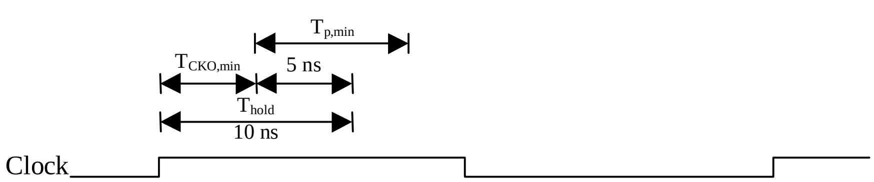
Q_1	Q_0	EN	Q_1^*	Q_0^*	MAX	J_1	K_1	J_0	K_0
0	0	0	1	0	0	1	1	0	0
0	0	1	0	0	0	0	0	0	1
0	1	0	0	1	1	0	0	0	0
0	1	1	1	0	1	1	1	0	1
1	0	0	0	1	1	1	1	1	0
1	0	1	1	1	1	0	0	1	1
1	1	0	1	1	1	0	0	1	0
1	1	1	0	0	1	1	1	1	1



4.



The minimum clock period of 32 ns (maximum clock frequency of 31.25 MHz). This is due to the worse case T_{CKO} (15 ns), inverter propagation delay (12 ns), & setup time (5 ns).



The fastest that the inverter could possibly be is $T_{hold} - T_{CKO,min} = 5$ ns. Because our fastest inverter has a 8 ns delay, we do not have to worry about that in the circuit. In order for the correct data to be propagated, $T_{CKO,min} + T_{p,min} > T_{hold}$