Professor Fearing **EECS 150/Problem Set 2** **Fall 1997**

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Problem 1 (25 pts)

a.

A	B	$G_{\rm in}$	$E_{\rm in}$	$G_{\rm out}$	$E_{\rm out}$	M
A	B	0	0	0	0	B
A	B	1	0	1	0	A
0	0	0	1	0	1	0
0	1	0	1	0	0	1
1	0	0	1	1	0	1
1	1	0	1	0	1	1
X	X	1	1	X	X	X

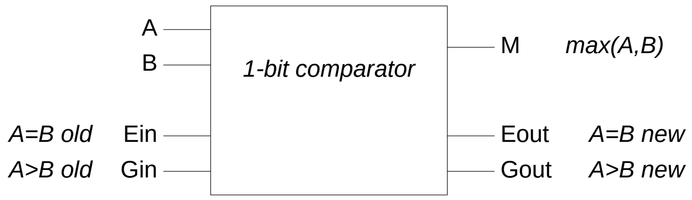
Logic equations :

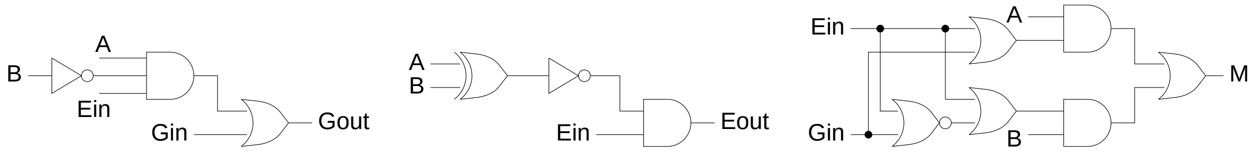
$$G_{\rm out} = G_{\rm in} + A\overline{B}E_{\rm in}$$

$$E_{\rm out} = E_{\rm in}(\overline{A}\,\overline{B} + AB) = E_{\rm in}\overline{(A \oplus B)}$$

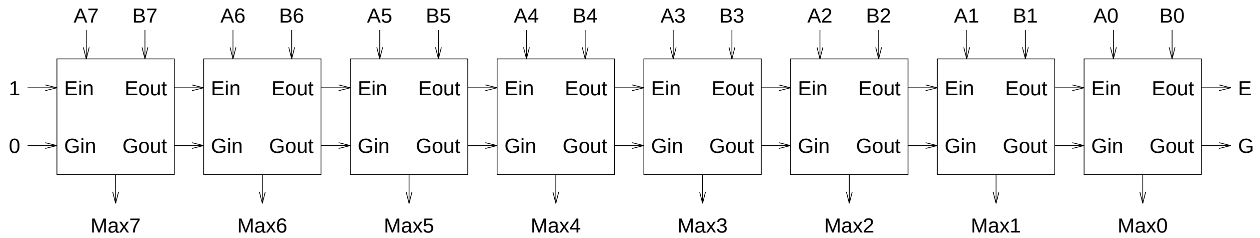
$$M = E_{\rm in}(A+B) + AG_{\rm in} + B\overline{G_{\rm in}}\,\overline{E_{\rm in}}$$

$$= A(E_{\rm in} + G_{\rm in}) + B(E_{\rm in} + \overline{G_{\rm in}}\,\overline{E_{\rm in}})$$



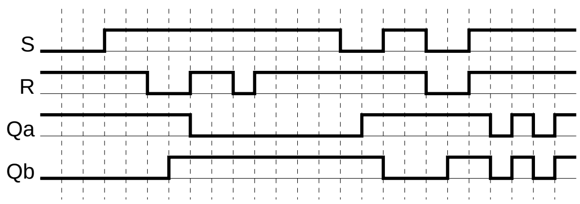


b.



c. The first comparator computes $E_{\rm out}$ and $G_{\rm out}$ in 3 gate delays (assuming all gates have unit delay, and an inverter delay is included). As the E signal propagates, each comparator adds onegate delay, so $E_{\rm in}$ at bit 0 arrives after 9 gate delays. All G signals are computed with two gate delays with respect to the corresponding $E_{\rm in}$ signal. Therefore the last comparator receives $G_{\rm in}$ after 10 unit delays and $E_{\rm in}$ after 9 gate delays. The final Max_0 output takes 4 more gate delays to compute. So the worst case delay of this circuit is 14 gate delays. Better times are possible using two level logic for the M function, and using an XNOR instead of inverter plus XOR.

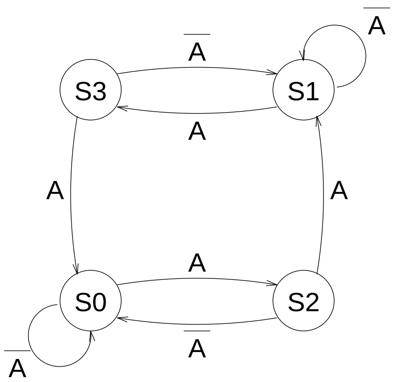
Problem 2 (25 pts)



At the end of the sequence the latch enters and leaves an illegal state due to the "00" input. As a result, it will start to oscillate.

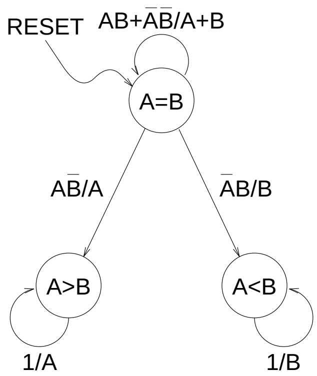
Problem 3 (25 pts)

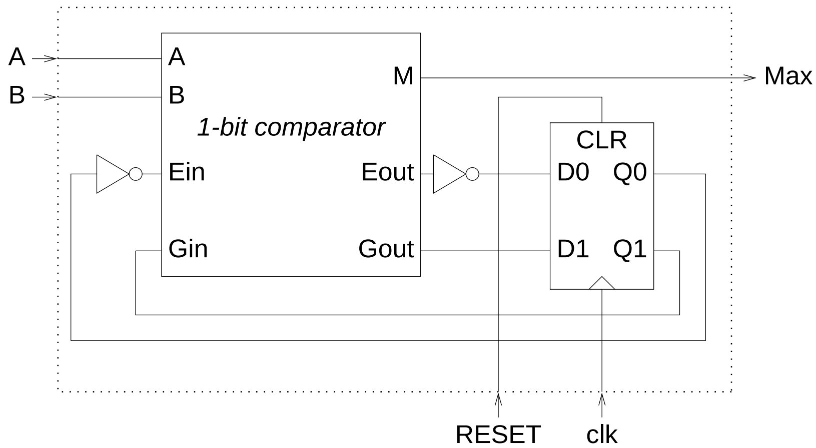
State	Q_0	Q_1	A	Next State	D_0	D_1
S0	0	0	0	S0	0	0
S0	0	0	1	S2	1	0
S1	0	1	0	S1	0	1
S1	0	1	1	S3	1	1
S2	1	0	0	S0	0	0
S2	1	0	1	S1	0	1
S3	1	1	0	S1	0	1
S3	1	1	1	S0	0	0



Problem 4 (25 pts)

A	B	State (Q_1Q_0)	Next State (D_1D_0)	Max
0	0	$A = B$ (00)	$A = B$ (00)	0
0	1	$A = B$ (00)	$A < B$ (01)	1
1	0	$A = B$ (00)	$A > B$ (11)	1
1	1	$A = B$ (00)	$A = B$ (00)	1
A	B	$A < B$ (01)	$A < B$ (01)	B
A	B	$A > B$ (11)	$A > B$ (11)	A





The comparator block is the same as the one from Problem 1 and the signals $\overline{E}$ and G can be used directly as state bits. Only three states are allowed. The "10" state results in undefined behavior and the Mealy FSM must be reset. The state register Flip-Flops are reset asynchronously using RESET.