University of California at Berkeley
College of Engineering
Department of Electrical Engineering and Computer Sciences

CS 150
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Lab 7/Checkpoint 1
Wire-Wrap and SRAMS

1 Objectives

For this lab, you will

1. Learn to use Wire-Wrap.
2. Gain more practice in digital design
3. Learn some strategies to test circuits
4. Wire an SRAM to the Xilinx on your Design Demonstration Board and test it.

2 Prelab

Following the directions in Section 3, use Wire-Wrap to connect a 61C64AH, an 8K $\times$ 8 SRAM to the Xilinx chip on your Design Demonstration Board. Use the pinouts in Figure 2 and a Wrap-ID from Page 4.

Design and `XMAKE` the control logic for the circuit described in Section 4.1.

3 Wire-Wrap

Wire-Wrap is a prototype construction technique where 30-gauge wire ("Wire-Wrap wire") is twisted around a square post to make a connection. These connections are physically strong, reliable, electrically sound, and quickly made.

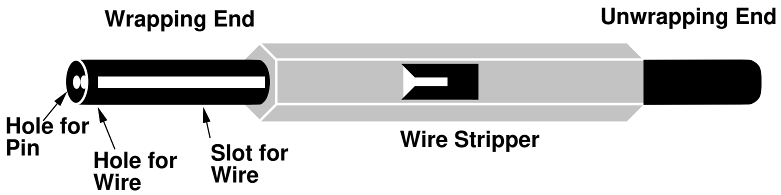
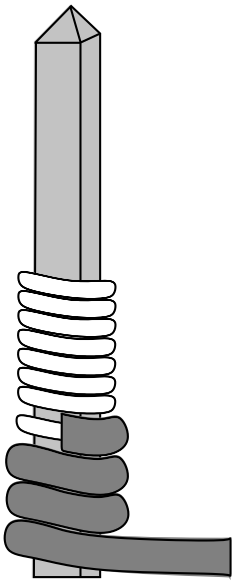


Figure 1: A Wire-Wrap tool (not to scale)

A Wire-Wrap tool consists of three parts:

- A central hexagonal rod with a wire stripper in the center (the little black notch).
- The wrapping end: a black circular rod with a hole in the center and an off-center hole leading to a side slot.
- The unwrapping end: a shorter circular rod with a hole in the center.

To make a Wire-Wrap connection,



1. Plan the route of your wire. Leave little slack, perhaps a half inch. Wires should lie flat against the board.

2. Cut the wire 2.5 inches longer than the route you chose.

3. Strip an inch of insulation off each end of the wire using the Wire-Wrap tool's stripper: thread the wire through the circular hole in the hexagonal handle, push it into the stripper's notch, and pull.

4. Insert a stripped end of the wire into the off-center hole in the end of the wrapping end of the tool. The wire should be visible in the slot on the side, although it should not hang out of this slot.

5. Put the wrapping end of the tool on the pin to be connected. The pin should fit easily in the center hole.

6. Gently, without pushing down or lifting up, twist the tool clockwise about twelve revolutions. This should wrap a few turns of insulated wire around the bottom, followed by the stripped wire. There should be a single layer of wire, with no spaces between turns.

If you make a mistake connecting a wire, remove it completely and start again. Place the unwrapping end of the tool on the pin and turn counter-clockwise. The wire should slide off. An unwrapped wire should not be re-wrapped.

Use differently-colored wire to group signals. For example, make the data lines in this lab green, the address lines orange, and the control signals red.

It is easy to forget that when you Wire-Wrap, the chip's pins appear as the *mirror image* of the usual pinout diagram. The best solution is to use a Wrap-ID, something that fits over the Wire-Wrap pins with the (correctly mirrored) pinout written on it. Such a Wrap-ID is printed on Page 4—cut it out, and carefully push it down on the pins before you start wiring your 61C64AH.

A few hints on wirewrapping:

- Always use Wrap-IDs. We will always provide you with Wrap-IDs, but if you ever need to wire wrap something and you don't have one, make one.

- Be neat. Although it is difficult to produce perfectly pristine connections, you should keep the wires as flat and as neet as possible. Messy wirewrap is much harder to debug, and is less reliable.

- Check for wire fragments. It is quite possible to have a little piece of wire fall down and short out two pins. Look carefully at the wires to make sure this does not happen.

- Inspect each connection after you make it, to insure it is to the right place and that the connection is solid. If you have a digital multimeter[1], use it to check each connection after you make it.

4 SRAMs

An SRAM (Static RAM) is a standard form of digital storage. It is generally faster, simpler, and more expensive then DRAM (Dynamic RAM). SRAMS are nice when one needs to store a moderate but not excessive amount of data, and needs to retrieve it quickly.

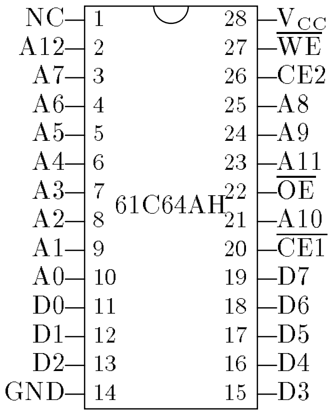
The 61C64AH you use is a high speed SRAM. It takes only 15 nanoseconds for an address to produce output data, and comes in a standard DIP package.

Their electrical interface is simple:

[1] If you don't, inexpensive ones are available at Radio Shack. You probably should buy one, they are good things to have.

- eight data pins, for input and output
- address input pins. The 61C64AH, a $2^{13} = 8192$-byte part, has 13 address pins.
- an active-low and an active high chip enable inputs ($\overline{\text{CE1}}$ and CE2), and an active-low output enable input ($\overline{\text{OE}}$)
- an active-low write enable ($\overline{\text{WE}}$).
- power (V_{CC}) and ground (GND) pins

In normal operation CE2 should be tied high. The $\overline{\text{CE1}}$ and $\overline{\text{OE}}$ inputs should be low to enable the chip and its output. If $\overline{\text{WE}}$ is high, the output lines always reflect the contents of the location specified by the address lines: change the address and the output will change. If $\overline{\text{WE}}$ is low, the data at the address will change to reflect the data input.



D0	72
D1	70
D2	69
D3	68
D4	67
D5	66
D6	65
D7	62
$\overline{\text{WE}}$	14

A0	10
A1	7
A2	5
A3	4
A4	3
A5	84
A6	83
A7	82
A8	81
A9	80
A10	79
A11	78
A12	77

Figure 2: 61C64AH Pinout (top view) and pins on the Xilinx

4.1 Testing the SRAM Wiring

There are generally two ways to test a memory, by producing specific patterns, or by a brute force approach. A set of specific patterns would test each wire a line at a time, to insure the output is correct. Brute force simply checks all possible values. For this lab, we recommend the brute force approach, as it is easier to implement. We will provide a bit file which tests the SRAM (how to use this file will be explained in the newsgroup), but you should also build your own version.

In addition to the wire wraps made to connect the SRAM, you need to connect the spare button to pin 58 and ground, so that you can use it in your design.

We provide a datapath for your test circuit `cs150:testsram.1`, but no control logic. The datapath is fairly straightforward. It consists of a 16 bit counter and an 8 bit LFSR. The lower 13 bits of the counter address the SRAM, and the LFSR data is output to the sram when the WE signal is asserted. When the WE signal is low, the contents of the SRAM are read in, and compared with the contents of the LFSR. These counters and flip flops have a synchronous reset, so reset must be high and the clock must come to reset them.

Your controller should write every memory location, and then read back all memory locations. It should clock the LFSR and the counter, to increment both the address and the LFSR. To write data, it should first make sure the address is stable, and on the NEXT clock cycle, assert the WE line. Once all the memory is full, both the counter and LFSR should be reset, and the data in the sram should be read back out of memory, and compared with the LFSR value. If the data is different at any time, you should assert ERROR and stop operation. Otherwise, just repeat the test forever. The reset button should reset your controller.

Name: ______________________ Name: ______________________

Lab Section (Check one)

M: ☐11 ☐12 T: ☐13 W: ☐14 ☐15 Th: ☐16

5 Checkoffs

1. Before you apply power to your Design Demonstration Board, show your TA your wiring. Your TA will then give you your SRAM

   SRAM wired to Xilinx TA: ____________(20%)

   SRAM wirewrapped reasonably neetly TA: ____________(15%)

2. Show your TA your SRAM test circuit, which you entered before lab.

   SRAM test circuit TA: ____________(10%)

3. Verify the SRAM is working by using the TA provided bit file.

   SRAM Tested TA: ____________(35%)

4. Verify the SRAM is working by using your design.

   SRAM Tested TA: ____________(10%)

5. Turned in on time TA: ____________(10%)

.... Cut Here ....

61C64AH

V_{CC}	NC
$\overline{WE}$	A12
CE2	A7
A8	A6
A9	A5
A11	A4
$\overline{OE}$	A3
A10	A2
$\overline{CE1}$	A1
D7	A0
D6	D0
D5	D1
D4	D2
D3	GND

61C64AH

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$\overline{OE}$	A3
A10	A2
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D6	D0
D5	D1
D4	D2
D3	GND

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$\overline{CE1}$	A1
D7	A0
D6	D0
D5	D1
D4	D2
D3	GND