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Fall 1996 | N. Weaver

Lab 6
Nasty Realities

1 Objectives

For this lab, you will

1. learn about crosstalk, shielding, and termination for long wires;
2. learn about different logic families and the affect of their slew rates; and
3. learn about "ground bounce" and bypass capacitors.

2 Prelab

All of the activity involved in this lab takes place in room 204B. Note that there is no way to earn extra credit for this lab other than turning it in on time, so read this writeup carefully so that you will know what to do when your lab section begins. If you are still confused, ask a TA *before* the start of your lab section.

3 Overview

Much of engineering is knowing what you can ignore. For example, we ignore the behavior of electrons in a digital circuit and think instead of 1's and 0's. This approximation has proven very successful, but it is important to know when we can no longer make it, or what to do to ensure we can make it.

Here are some of the assumptions we have been making:

- Wires are ideal: at any point in time, the voltage at every point on the wire is the same.
- There are exactly two logic levels: high and low.
- The power supply's voltage is constant.

In this lab, you will see these assumptions fail and learn how to avoid it.

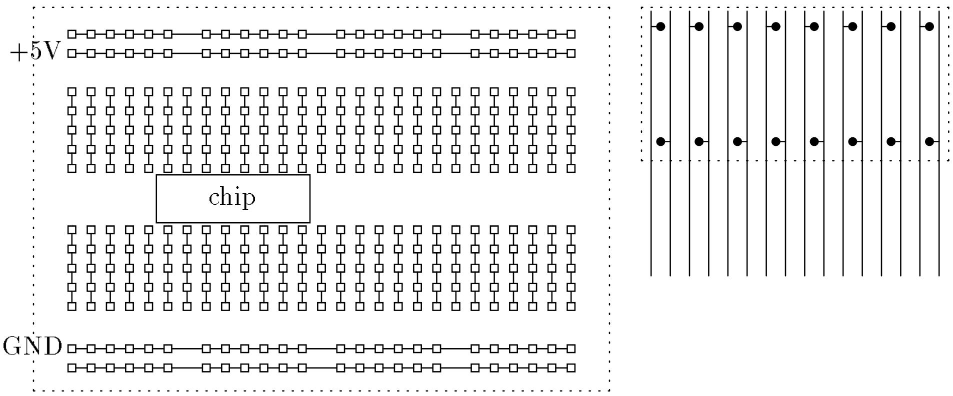
This lab is broken into two large experiments. Section 5 discusses the nasty realities of wires; Section 5.4 describes the associated experiment. Section 6 discusses the nasty realities of supplying power; Section 6.1 describes the associated experiment. Section 4 describes some miscellaneous things you need to know to build the circuits in this lab.

4 Details

4.1 Breadboard

We will use a breadboard—a slab of plastic covered with holes connected by hidden metal contacts—to build the circuits for this lab. Pushing stripped ends of wire, leads of discrete components, or IC pins into these holes connects them electrically to anything in a hole in the same column.

The connections inside the breadboard are shown in Figure 1a. Use the rows of connected holes for power and ground, the columns for your circuit. (Note that there is a break in the rows between the left



(a) (b)

Figure 1: (a) Breadboard connections. (b) Ribbon cable DIP plug.

and right halves of the boards.) Put chips horizontally in the wide space separating the two columns of connections. Their pins should fit in the lowest row of the upper columns and the upper row of the lower columns.

Power the circuits in this lab with the power supply we have used to power the Xilinx boards. Connect it to the banana jacks attached to the breadboard, and run wires from the jacks to the breadboard's power rows. Clamp the wires to the jacks by unscrewing the top of the jack, threading a stripped wire end into the exposed hole, and screwing down the top of the jack.

4.2 Ribbon Cable

Some of the circuits in this lab use a long (ten foot) ribbon cable, a flat strip of insulated parallel wires. Adjacent wires in the cable alternate between connecting to the top and bottom pins of a 16-pin DIP connector, as shown in Figure 1b.

4.3 Resistors and Capacitors

Discrete resistors, which you will be using in this lab, are marked with a code consisting of three colored bands[1]. Each color corresponds to a number, as listed below:

Black	Brown	Red	Orange	Yellow	Green	Blue	Violet	Grey	White
0	1	2	3	4	5	6	7	8	9

The first two bands represent the first two digits of the resistance, and the third represents the number of zeros following the first two numbers. For example, a resistor labeled yellow violet red is

$$\underbrace{4}_{\text{yellow}}\ \underbrace{7}_{\text{violet}}\ \underbrace{00}_{\text{red}=2}\ \Omega = 4.7\text{K}$$

Capacitors are labeled similarly, although usually with three digits rather than colored bands. The number you obtain is the number of *pico*farads. For example, a capacitor labeled "104" is

$$\underbrace{1}_{1}\underbrace{0}_{0}\underbrace{0000}_{4}\text{pF} = 0.1\mu\text{F}$$

[1] Actually, they usually have a fourth band, indicating tolerance, and perhaps even a fifth, indicating reliability.

5 Wires

The nasty reality of wires is that they have "parasitic" resistance, capacitance, and inductance. Usually, these so-called parasitics are small enough to ignore, but when a wire is very long, or when a very high-speed signal is being applied, their effects can dominate.

Figure 2 is a model of these parasitics. The resistors are due to the wire conducting imperfectly, the capacitors are due to nearby conductors, and the inductors are due to current in the wire producing a magnetic field.

The parasitic capacitance slows a wire's response to a sudden change in voltage, and the parasitic inductance slows the response to a sudden change in current. Most digital logic lines conduct little current, but require the voltage to change frequently. Power supply lines have the opposite problem: their voltage is constant, but when many things change suddenly (e.g., when the clock rises), a sudden burst of current is required.

Together, inductance and capacitance make the wire behave as a *transmission line*, making signals travel along the wire rather than being instantly broadcast. This is unimportant at low frequencies, but can become a problem at high frequencies.[2]

The resistance is due to the wire being an imperfect conductor. At high currents, such as those on power wires, this can become a problem. At high frequencies, the resistance coupled with the inductance and capacitance forms a filter, causing the signal to "smear" as it travels along the wire.

5.1 Termination

Reflections are a big problem in transmission lines. Like water waves reflect on the side of a swimming pool, signals traveling along a transmission line can reflect at the end of a wire and interfere constructively, causing large voltage spikes.

Proper termination can eliminate reflections. Connecting a resistor with a value equal to the characteristic impedance of the transmission line[3] is the simplest form of termination. Like waves on the ocean, this causes signals traveling along the transmission line to "crash on the beach"—dissipate in the resistor.

5.2 Capacitive Coupling

There is capacitance between any two conductors, and wires running near each other are no exception. Figure 3 shows a model of capacitive coupling among three wires. Closer wires, in general, have more capacitance than farther-apart wires.

Capacitors tend to keep the voltage between their terminals constant. This effect can induce a voltage/current spike on anything capacitively coupled when the voltage on a wire changes suddenly.

The capacitance between two conductors increases as they grow nearer and their common area increases. Thus, two long wires running parallel have more capacitive coupling than two short wires running orthogonally. This is unfortunate, since we often want to run many long wires near each other: most cables are like this.

[2] The speed of light, just under a foot per nanosecond, is a fundamental limitation. The clock period of today's 100MHz digital circuits is just ten nanoseconds.

[3] Ribbon cable and twisted pair have a characteristic impedance of about 100Ω. RG-58 coaxial cable, which we used to connect the signal generator to the oscilloscope in an earlier lab, has a characteristic impedance of 50Ω. This is what the pulse generator expects to be driving, incidentally. RG-59 coaxial cable, used for video, is 75Ω.

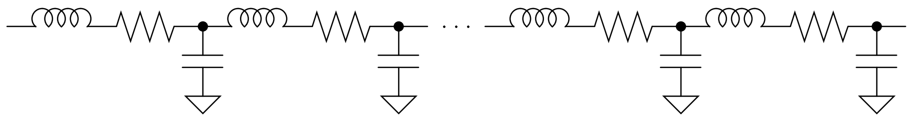


Figure 2: A more realistic model of a wire

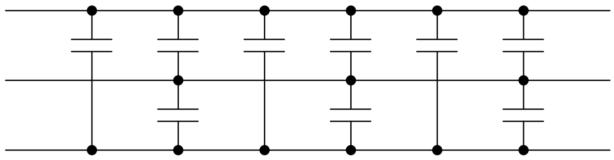
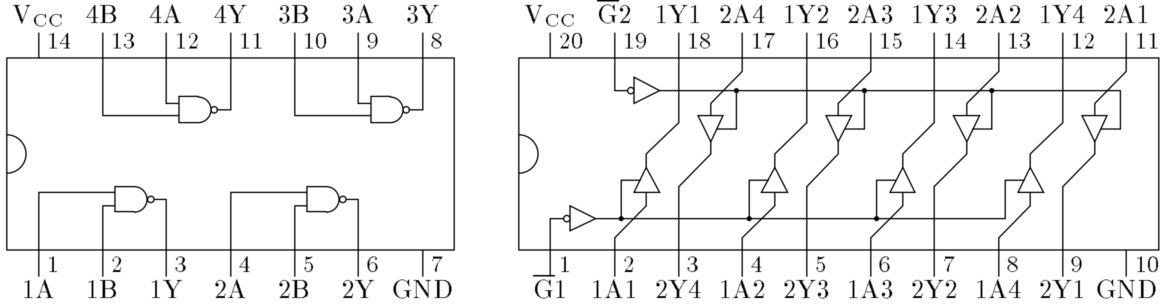


Figure 3: Capacitive coupling among three wires



(a) the 74x00

(b) the 74x244

Figure 4: Pinouts

5.3 Shielding

Shielding, surrounding a wire with a grounded conductor, eliminates capacitive coupling. Coaxial cable is fully shielded: it consists of a central conductor for the signal surrounded by an insulator completely surrounded by a conductor—the shield. The problem with using coaxial cables for everything is that they are big and expensive.

Fortunately, incomplete shielding is often enough. Placing a grounded wire between two signal-carrying wires is a simple form of incomplete shielding that works well in practice.

5.4 To Do

We will look at transmission line and coupling behavior in a ten-foot section of ribbon cable using the circuits of Figure 5. We will experiment with three logic families (LS, C, and F), and with two ways of reducing coupling and transmission line effects.

The LS logic family is a fairly old, traditional family based on bipolar transistors. The C family is very slow, low-power CMOS. The F family is very fast and power-hungry, also based on bipolar transistors. Chips in these families have the same pinouts and work with +5V power supplies.

1. Build the circuit in Figure 5a on the breadboard. Use a 74LS00, whose pinout is shown in Figure 4a, to drive a 1MHz, 5V square wave from the pulse generator along the ribbon cable. The 50Ω resistor presents a load to the pulse generator so the voltage you set is the voltage you get.

   Make a second NAND gate constantly drive a logic 1 onto an *adjacent* wire. Look at Figure 1b and read Section 4 to determine how the wires in the ribbon cable connect to pins.

2. Using the oscilloscope, observe the wires labeled "Square Wave" and "1" in Figure 5a. Observe them at the end *away from the 74LS00!* Both should be very "ringy" square waves.

   Measure the highest and lowest voltage you observe on the two signals, accurate to half a volt, and enter them in the 74LS00 column of Table 1a.

3. Disable the Pulse Generator and disconnect the power. Remove the 74LS00 and replace it with a 74C00. They have the same pinout and function.

   Reconnect the power and reenable the Pulse Generator. Measure the highest and lowest voltages on the "Square Wave" and "1" wires as before and enter them in the 74C00 column of Table 1a.

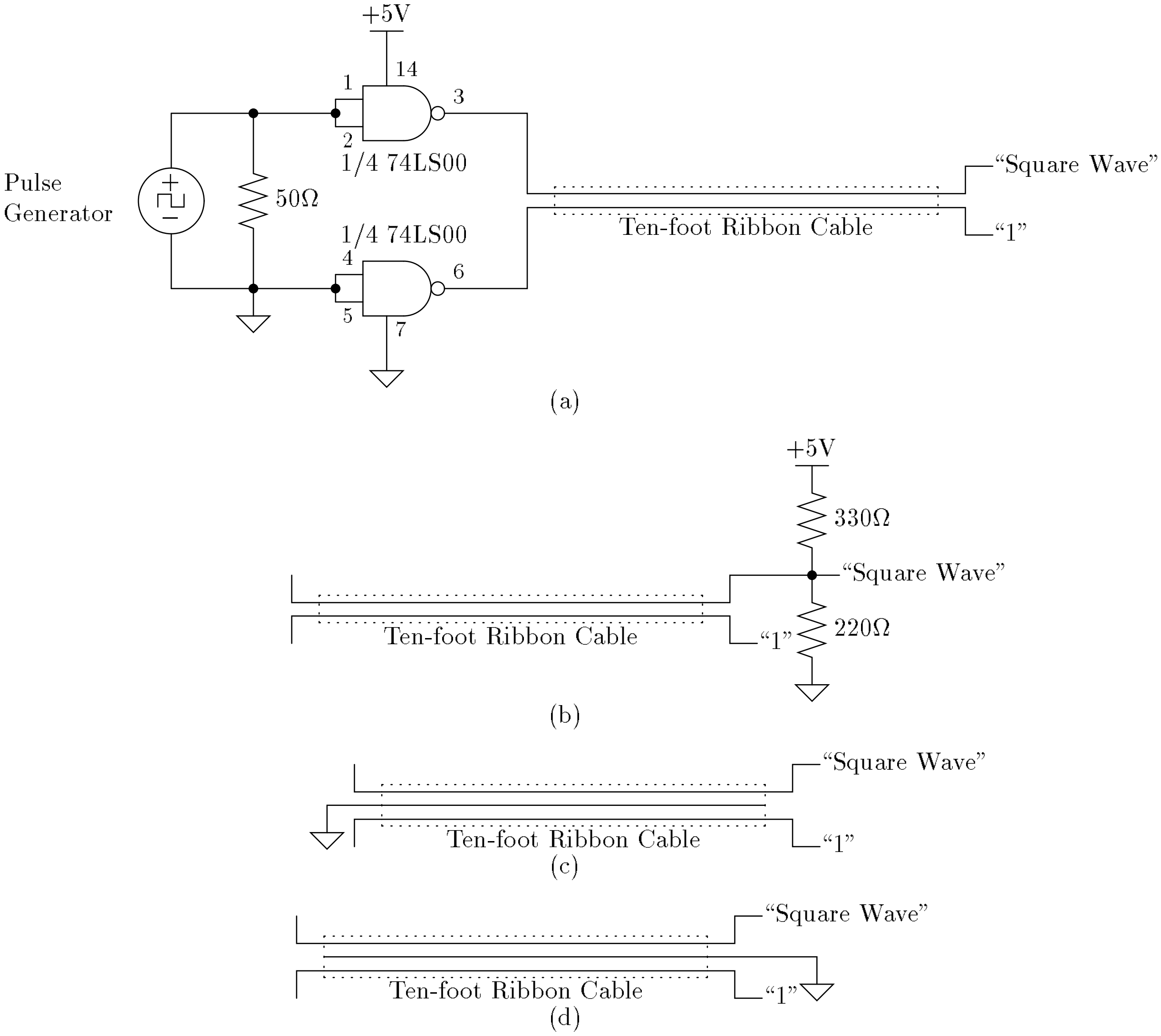


Figure 5: Test Circuits for the Ribbon Cable. (a) Adjacent wires. (b) Terminating the signal. (c) Using a shield, source grounded. (d) Using a shield, destination grounded.

4. Power down the circuit, replace the 74C00 with a 74F00, and repeat the experiment. Record the results in the 74F00 column of Table 1a.

5. Power down the circuit and switch back to the 74LS00. Terminate the ribbon cable using two resistors as shown in Figure 5b. Measure the highest and lowest voltage as before and enter them in the Terminated column of Table 1b.

6. Remove the termination and introduce a "shield" wire between the "Square Wave" and "1" wires by moving the connection to the "1" wire.

   Ground the source end as shown in Figure 5c and measure the high and low voltages on the two signals. Enter them in the Source column of Table 1b.

   Remove the ground on the source end and ground the destination end as shown in Figure 5d. Measure the high and low voltages and enter them in the Destination column of Table 1b.

7. Use your results to fill in Table 1, and answer the questions below it.

6 Power

Every wire in a circuit has some capacitance to ground, either due to coupling or from gate inputs. Changing the voltage on this wire, therefore, requires charging or discharging this capacitance. This requires a current proportional to the capacitance and the charging speed,

$$I = C\frac{dV}{dt},$$

so changing the voltage quickly (i.e., dV/dt large) or charging a large capacitance requires high current.

The current for charging or discharging must come from somewhere. The power supply is the obvious candidate, since it is designed to supply as much current as necessary to maintain a constant voltage on the power lines. However, it is separated from the circuitry by long wires, which have a significant inductance.

The nasty reality of power: the inductance on the power lines tends to keep the current constant, and will cause the voltage (the power supply voltage!) to change to reduce the change in current. This effect is often called "ground bounce" because the voltage on the ground line can suddenly spike.

A solution to this problem is to liberally sprinkle 0.1μF "bypass" capacitors around the circuit, usually one per chip. These can briefly supply enough current to allow the power supply time to "catch up."

6.1 To Do

We will simulate a heavily-loaded bus by driving seven 50pF loads from a 74LS244 octal bus driver. We will observe the effects of this on the outputs and an eighth output that should be a constant logic 1.

Build the circuit in Figure 6 on the breadboard using a 74LS244, whose pinout is in Figure 4b. Tie seven of the inputs to a 1MHz square wave from the pulse generator and connect their outputs through seven 50pF capacitors to ground. Tie the eighth input high. Observe its output and one of the loaded outputs on the oscilloscope.

1. Measure the risetime t_{LH} and falltime t_{HL} of one of the loaded outputs. Risetime and falltime are measured as the times between the 10% and 90% points on the voltage curve. Try for two significant digits. Record these in the Simple column of Table 2a. Measure the highest and lowest voltages you observe on the unloaded output and record them in the same column.

2. Make things worse by connecting a 10μH inductor in series with the +5V power supply wire. Repeat the measurements, recording your results in the "10μH on power" column.

3. Make things better by connecting a 0.1μF capacitor across the power and ground pins of the '244. Repeat the measurements and record your results in the "with bypass" column.

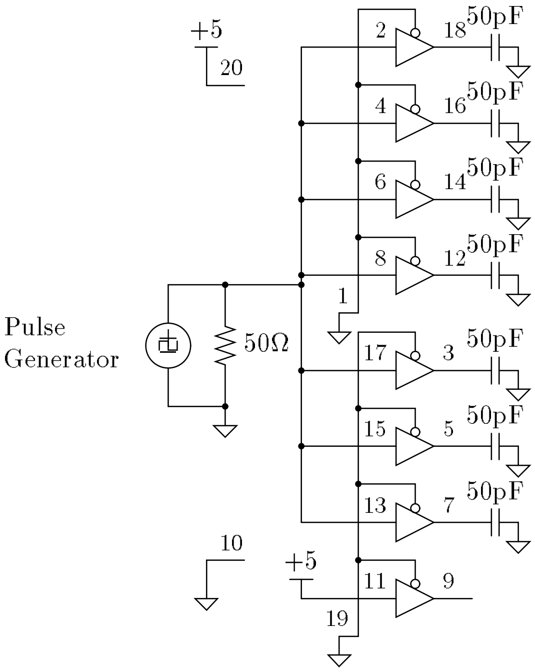


Figure 6: Circuit for Power Experiments

4. Power down the circuit, replace the 74LS244 with a 74F244, and fill in Table 2b using the same procedure.

5. Add a second 0.1μF bypass capacitor and observe the result. Fill in Table 2, and answer the questions below it.

		74LS00	74C00	74F00
"Square	V_{HIGH}			
Wave"	V_{LOW}			
"1"	V_{HIGH}			
	V_{LOW}			

(a)

			Grounded Shield	
		Terminated	Source	Destination
"Square	V_{HIGH}			
Wave"	V_{LOW}			
"1"	V_{HIGH}			
	V_{LOW}			

(b)

Which logic family (LS, C, or F) exhibited the worst coupling? The best? Why?

Which works better to reduce coupling, termination or shielding? Which form (source or destination) of shielding works better? Why might this be the case?

Table 1: Table of Results for the Ribbon Cable Circuits. (a) Different logic families. (b) Effect of termination and shielding with the 74LS00.

		74LS244		
		Simple	10μH on power	with bypass
Loaded	t_{LH}			
Output	t_{HL}			
“1”	V_{HIGH}			
	V_{LOW}			

(a)

		74F244		
		Simple	10μH on power	with bypass
Loaded	t_{LH}			
Output	t_{HL}			
“1”	V_{HIGH}			
	V_{LOW}			

(b)

Which logic family (LS or F) needs bypassing more? Why?

Does adding a second bypass capacitor help? Why or why not?

Table 2: Table of Results for the Power Experiment. (a) 74LS244 (b) 74F244

Name: ________________________ Name: ________________________

Lab Section (Check one)

M: ☐11 ☐12 T: ☐13 W: ☐14 ☐15 Th: ☐16

7 Checkoffs

1. Table 1a completed TA: ____________(20%)
2. Table 1b completed TA: ____________(20%)
3. Questions in Table 1 answered TA: ____________(10%)
4. Table 2a completed TA: ____________(20%)
5. Table 2b completed TA: ____________(20%)
6. Questions in Table 2 answered TA: ____________(10%)
7. Turned in on time TA: ____________(10%)

Game Over, man! Game Over.