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CS 150
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Checkpoint 5, The Final Frontier
IR Reciever

1 Objectives

For this checkpoint, you will

1. Build the low and high level interface to recieve over the Infra Red link
2. Build and implement the CRC check on the reciever
3. Bask in the glory of your now working project.

2 Introduction

In this checkpoint you will add the last component to your design, the IR reciever, as well as wire up the actual hardware to send and recieve bits. With this, your project will be working completely, except for any extra credit (to be discussed next week) you may wish to contemplate.

3 IR reciever

The IR reciever operates on a basis similar to your UART reciever, but with a few key exceptions. To begin with, it operates at 16 times the bit clock, not 8 times. And the encoding is more complex. In order to caputure data, the serial line must be sampled at both cycle 4 and cycle 12. If it is high at cycle 4 only, the bit is a 0. If it is only high on cycle 12, the bit is a 1. If both are low, then there is no data to recieve, and the reception is aborted. If both are high, a collision is signaled and reception is aborted. Also, while the IR line is low for a continued period of time, the reciever asserts OKTOSEND so that the IR sender knows that the air is clear.

In order to synchronize properly, the sender first sends the bit string 01010101 as the prolog, and then the rest of the data. So the first bit recieved is a 0, and if this pattern is recieved, the reciever continues to recieve the other 128 bytes of data.

4 Interaction with the computer

Since the serial link is much slower then the IR link, we use 16 buffers to store recieved packets. Both the IR reciever and the computer sender will have a counter which indicates what buffer to fill. Thus, there is a producer/consumer relationship between the IR reciever and the computer sender. However, sometimes we don't pass a packet on to the computer. The first is when only a partial packet is recieved. The second is when the packet is for a different board. (The 4 bit board ID should be specified by 4 DIP switches). Look at the high level description to determine where this occurs in the packet. The third is when the CRC check fails. It all these cases, the reciever should not increment its pointer and should not tell the computer sender that another packet is available.

THe reciever should be operating at all times, and thus you can test things by using a mirror. We will provide an FTP program which can be used to transfer a file between machines on the IR network.

Also present are base station repeaters. If you aim your transmitter and reciever carefully at the repeaters, the packet will be broadcast through all recievers on the lab bench

5 Physical Transmitter/reciever

There is a nice standard reciever which your TA will issue for your use. It fits on top of the pins on the demoboard area, and you can wire wrap your connections underneeth. THe reciever line should be connected to pin 6 on your xilinx board. THe reciever is ACTIVE LOW!

There is also an active low sender which you have to build using a hex inverter chip, a resistor, a capacitor, and an LED. The circuit diagram is below, and it should be hooked up to pin 8 on your xilinx. The inverter is used to power the LED transmitter. The LED mounts in the same way as the reciever, while the other parts should be inserted in the back of your board. (The flat spot on the LED indicates direction.) The A pins are the inputs to the 6 inverters, and the Y pins are the output.

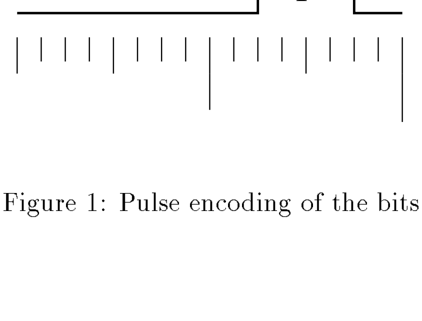

Figure 1: Pulse encoding of the bits.

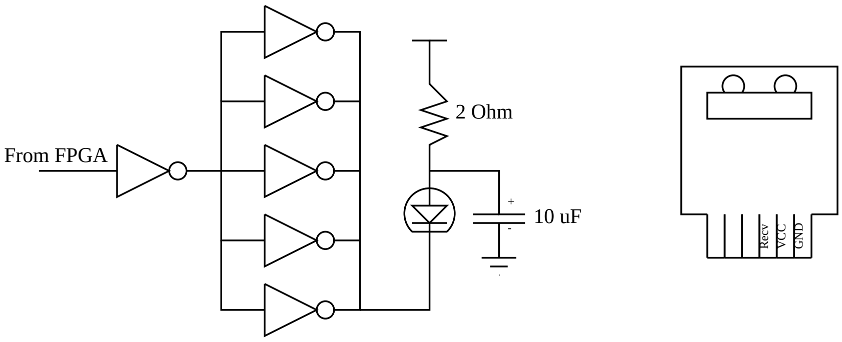

Figure 2: Transmitter schematic and reciever connections.

Name: ____________________ Name: ____________________

Lab Section (Check one)

M: ☐11 ☐12 T: ☐13 W: ☐14 ☐15 Th: ☐16

6 Checkoffs

1. Correct recieves over IR TA: ____________(40%)

2. Complete integration of everything TA: ____________(50%)

3. Turned in on time TA: ____________(10%)

.... Cut Here ....

7404		7404		7404		7404		7404	
VCC	1A	VCC	1A	VCC	1A	VCC	1A	VCC	1A
6A	1Y	6A	1Y	6A	1Y	6A	1Y	6A	1Y
6Y	2A	6Y	2A	6Y	2A	6Y	2A	6Y	2A
5A	2Y	5A	2Y	5A	2Y	5A	2Y	5A	2Y
5Y	3A	5Y	3A	5Y	3A	5Y	3A	5Y	3A
4A	3Y	4A	3Y	4A	3Y	4A	3Y	4A	3Y
4Y	GND	4Y	GND	4Y	GND	4Y	GND	4Y	GND