University of California at Berkeley
College of Engineering
Department of Electrical Engineering and Computer Sciences
Computer Science Division

CS 150 — J. Wawrzynek
Fall 1996 — Handout #1

Digital Design
Course Information and Itinerary

Revision Date: August 27, 1996

Instructor: John Wawrzynek, Associate Professor
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office hours: Tu 1:00–2:00pm & 4:00–5:00pm, Th 1:00–2:00pm

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Course Description:
Overview of synchronous digital system design. System clocking, design of combinational logic and finite state machines. Schematic entry and simulation using computer aided design tools. Implementation with MOS and logic families. Datapaths and controllers in microprocessors. System design using programmable and reconfigurable logic components. Prototyping, instrumentation, and debugging techniques.
The course includes software exercises to introduce the fundamentals of computer based design tools, as well as a traditional "hand-on" hardware laboratory including a substantial final project. Students will receive access to the Intel computers in 123 Cory and to the hardware laboratory in 204B cory.
The textbook used will be *Contemporary Logic Design*, R. H. Katz, Benjamin/Cummings Publishing Co.

Class Communications:
All class information will be stored online, available through links from the class homepage at `http://www-inst.eecs.berkeley.edu/~cs150/`. Check there for class notes, homework assignments, lab exercise handouts, and all other class materials. For notices and announcements we will post messages to the CS150 newsgroup or send email to individuals. **It is your responsibility to check your email and the class newsgroup at least once every day.** We will assume that you will see our postings within 24 hours of their appearance.

Tentative Course Schedule:

Week	Day	Lecture	Reading
1	No Lab		
	Tu 8/27	Course Introduction	Ch. 1
	Th 8/29	Digital Signal Representations	
2	Lab1: Introduction to Schematic Entry and Simulation		
	Tu 9/3	Combinational Logic, State Elements	
	Th 9/5	Finite State Machines	
3	Lab2: Schematic Entry and Simulation II, Finite State Machine		
	Tu 9/10	Implementation Technology Overview	
	Th 9/12	FPGA Overview	Xlinix Arch. in Reader
4	Lab3: FPGA I, FSM		
	Tu 9/17	Interconnections	
	Th 9/19	Memory	
5	Lab4: Instrumentation		
	Tu 9/24	Design Example: Network Switch	
	Th 9/26	Exam Review	
6	Lab5: FPGA II, Logic Elements		
	Tu 10/1	MIDTERM I	
	Th 10/3	CMOS Circuits, Timing, and Noise	
7	Lab6: Nasty Realities		
	Tu 10/8	Boolean Algebra Basics	Ch. 2
	Th 10/10	Two-level Logic	
8	Lab7: RAM Interfacing		
	Tu 10/15	Multi-level Logic	Ch. 3
	Th 10/17	Simplication, Hazards	
9	Project Checkpoint 1		
	Tu 10/22	Arithmetic Circuits, Adders	Ch. 5
	Th 10/24	ALUs, Shifters	
10	Project Checkpoint 2		
	Tu 10/29	Multipliers	
	Th 10/31	Sequential Circuits	Ch. 6
11	Project Checkpoint 3		
	Tu 11/5	Asychronous Inputs	
	Th 11/7	Self-timed circuits	
12	Project Checkpoint 4		
	Tu 11/12	FSMs revisited	
	Th 11/14	Optimization	
13	Project Checkpoint 5		
	Tu 11/19	Exam Review	
	Th 11/21	MIDTERM II	
14	No Checkpoint Due		
	Tu 11/26	Spare, TBA	
	Th 11/28	Thanksgiving	
15	Final Project Checkoff		
	Tu 12/3	Spare, TBA	
	Th 12/5	Course recap and exam review (Final Lecture)	
16	Tu 12/10		
	Th 12/12	FINAL EXAM 12:30–3:30	
17	Tu 12/17		
	Th 12/19	Final Grades Posted	